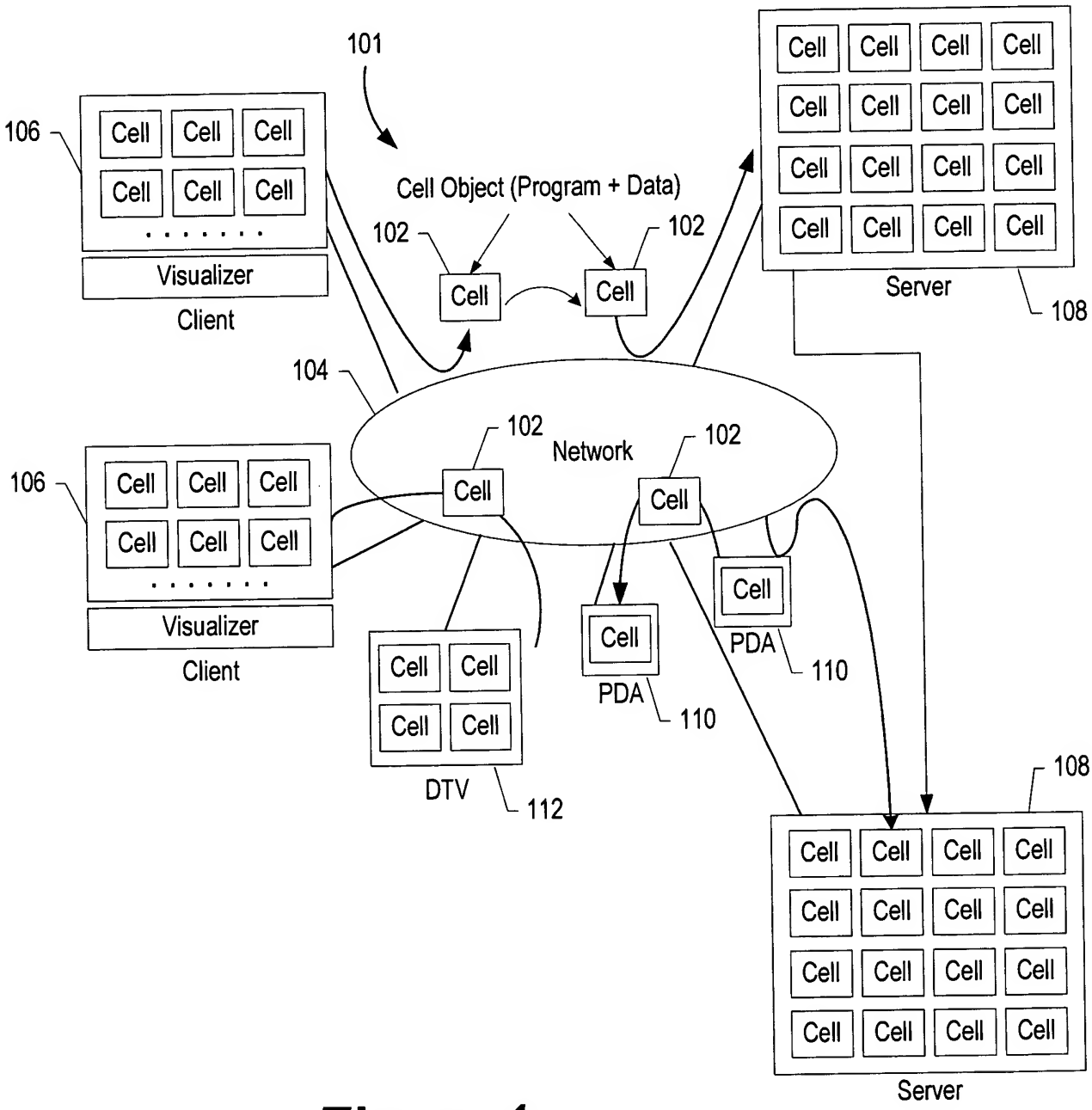
101
106
Cell
Visualizer
Client
Cell Object (Program + Data)
102
Cell
Server
108
104
Network
PDA
110
DTV
112

Figure 1

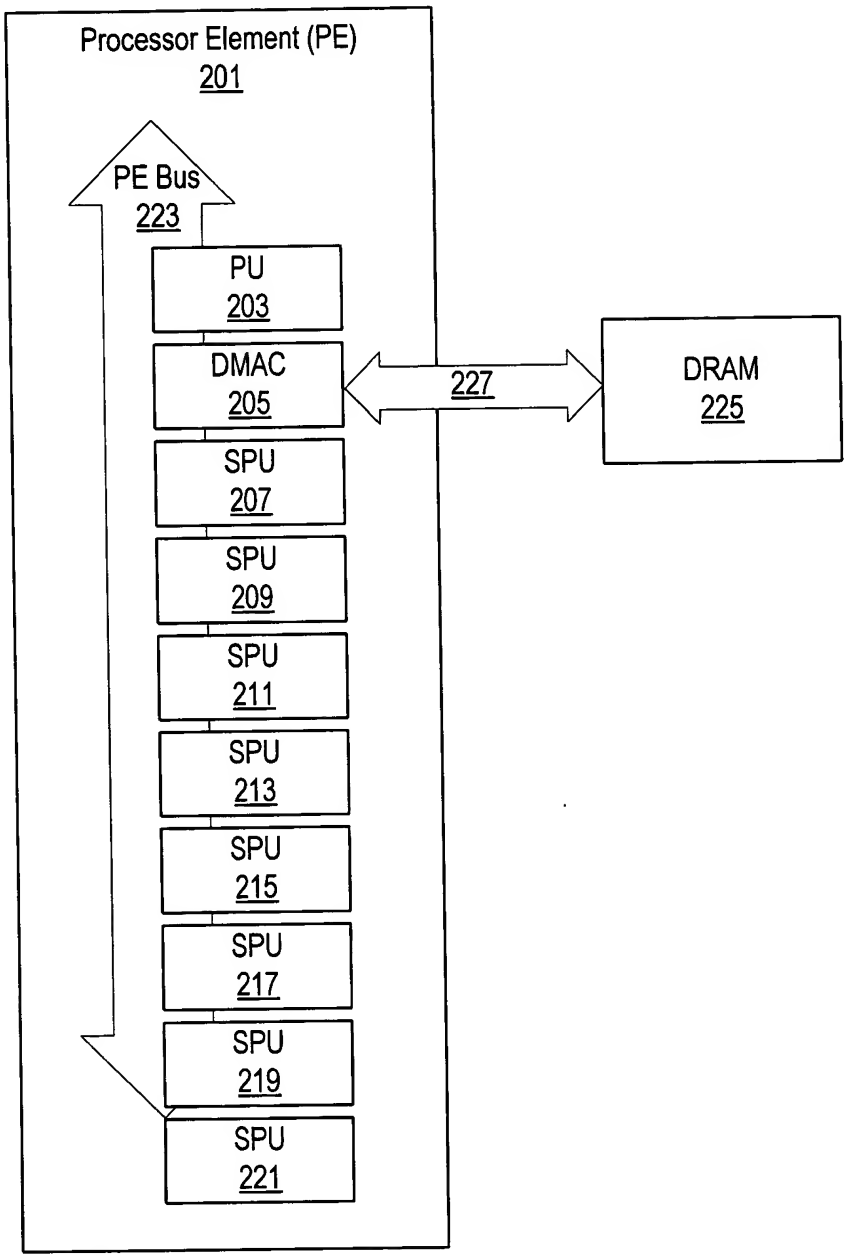
Processor Element (PE)
201
PE Bus
223
PU
203
DMAC
205
227
DRAM
225
SPU
207
SPU
209
SPU
211
SPU
213
SPU
215
SPU
217
SPU
219
SPU
221

Figure 2

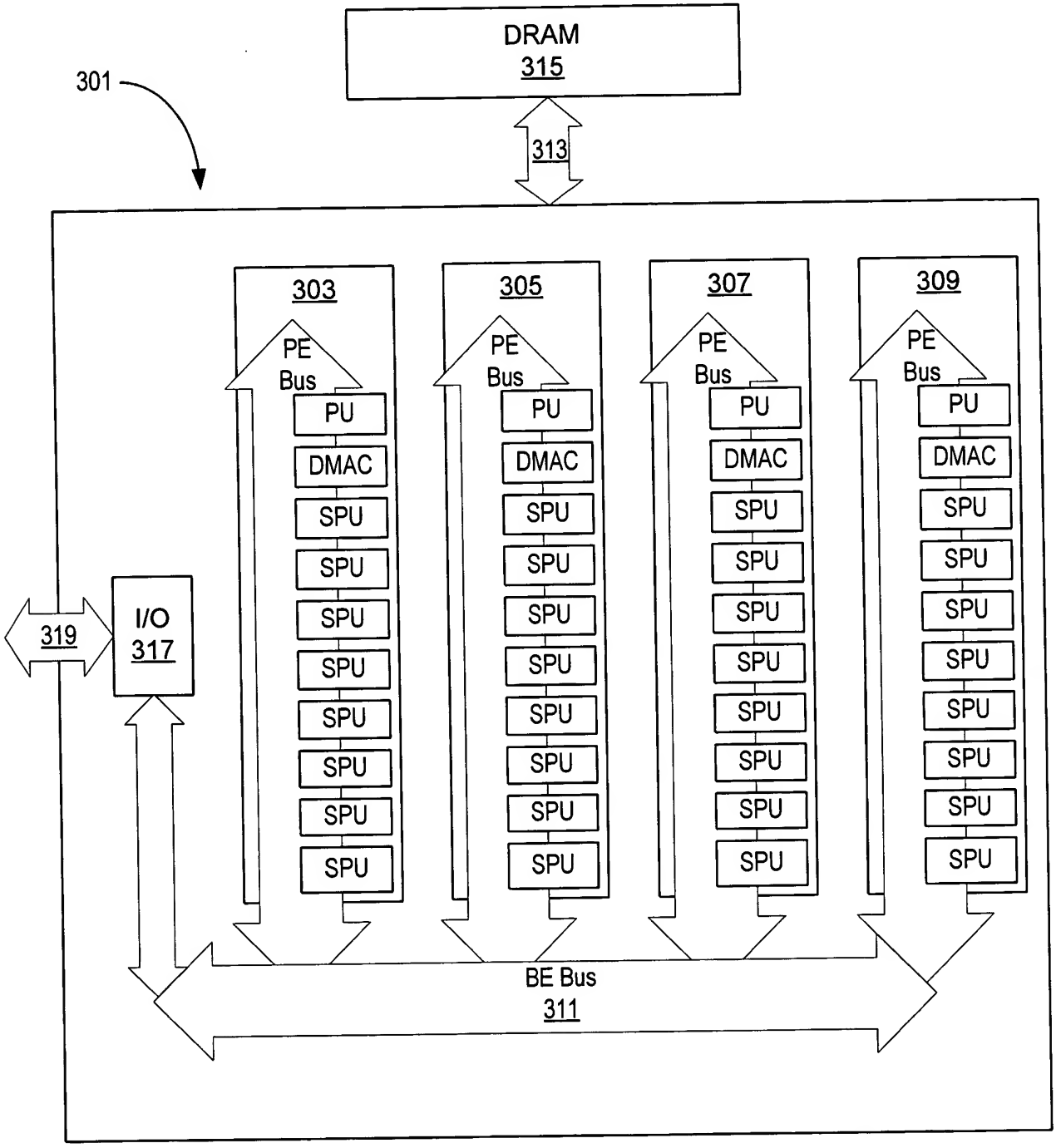
DRAM
315
301
313
303
305
307
309
PE
Bus
PU
DMAC
SPU
I/O
317
319
BE Bus
311

Figure 3

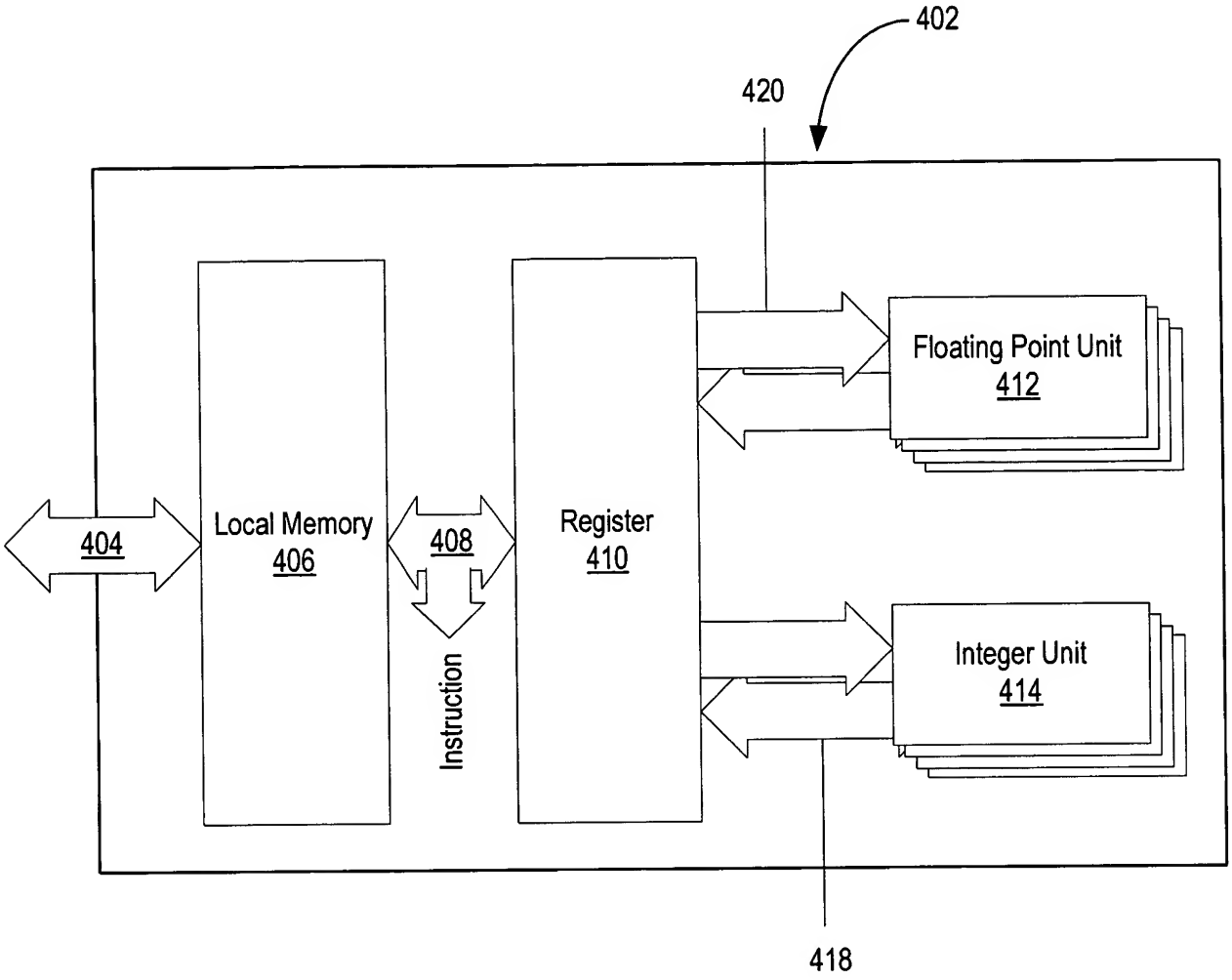
402
420
Floating Point Unit
412
Local Memory
406
404
408
Register
410
Instruction
Integer Unit
414
418

Figure 4

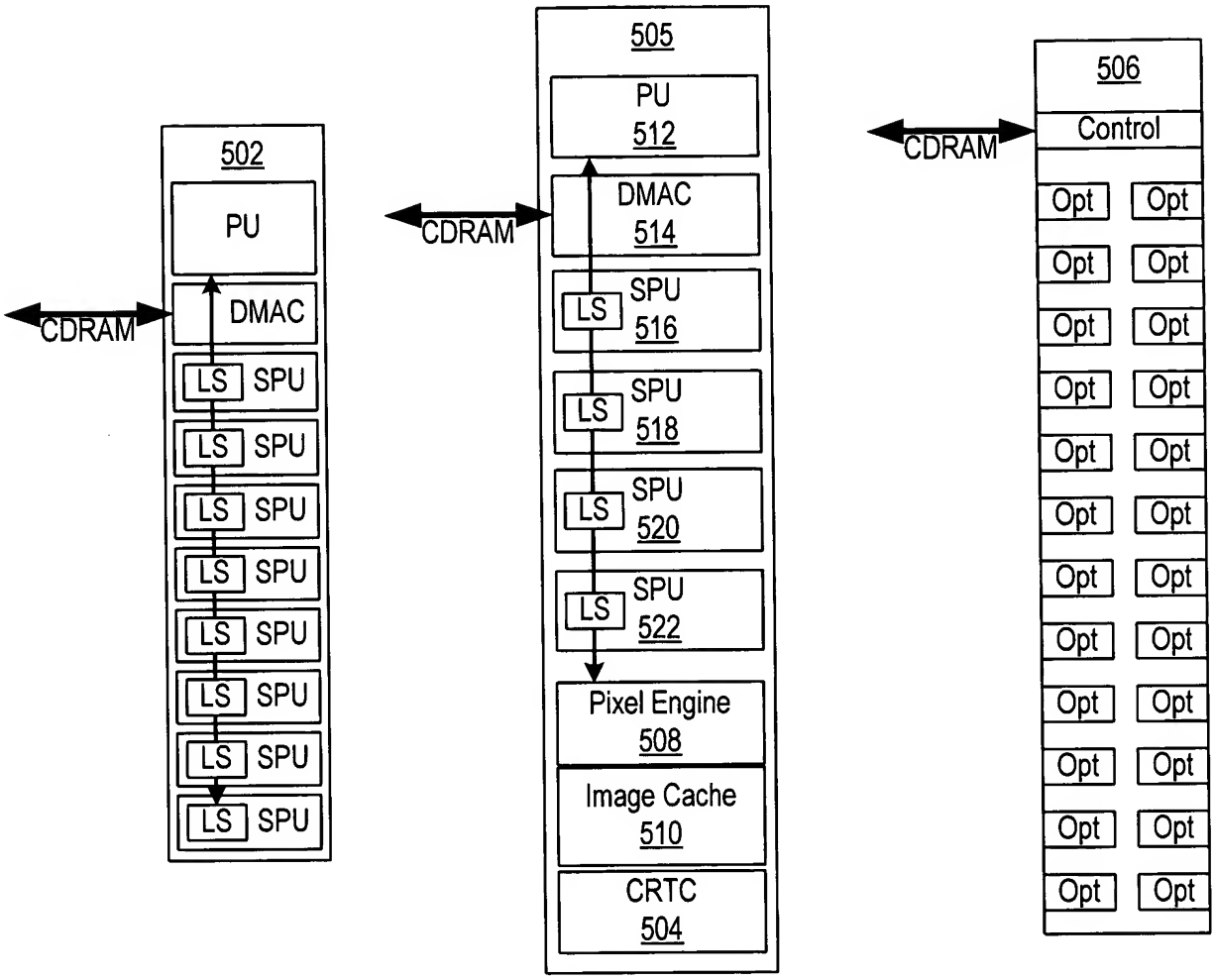
502
PU
DMAC
CDRAM
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
505
PU
512
DMAC
514
CDRAM
SPU
516
SPU
518
SPU
520
SPU
522
Pixel Engine
508
Image Cache
510
CRTC
504
506
Control
CDRAM
Opt

Figure 5

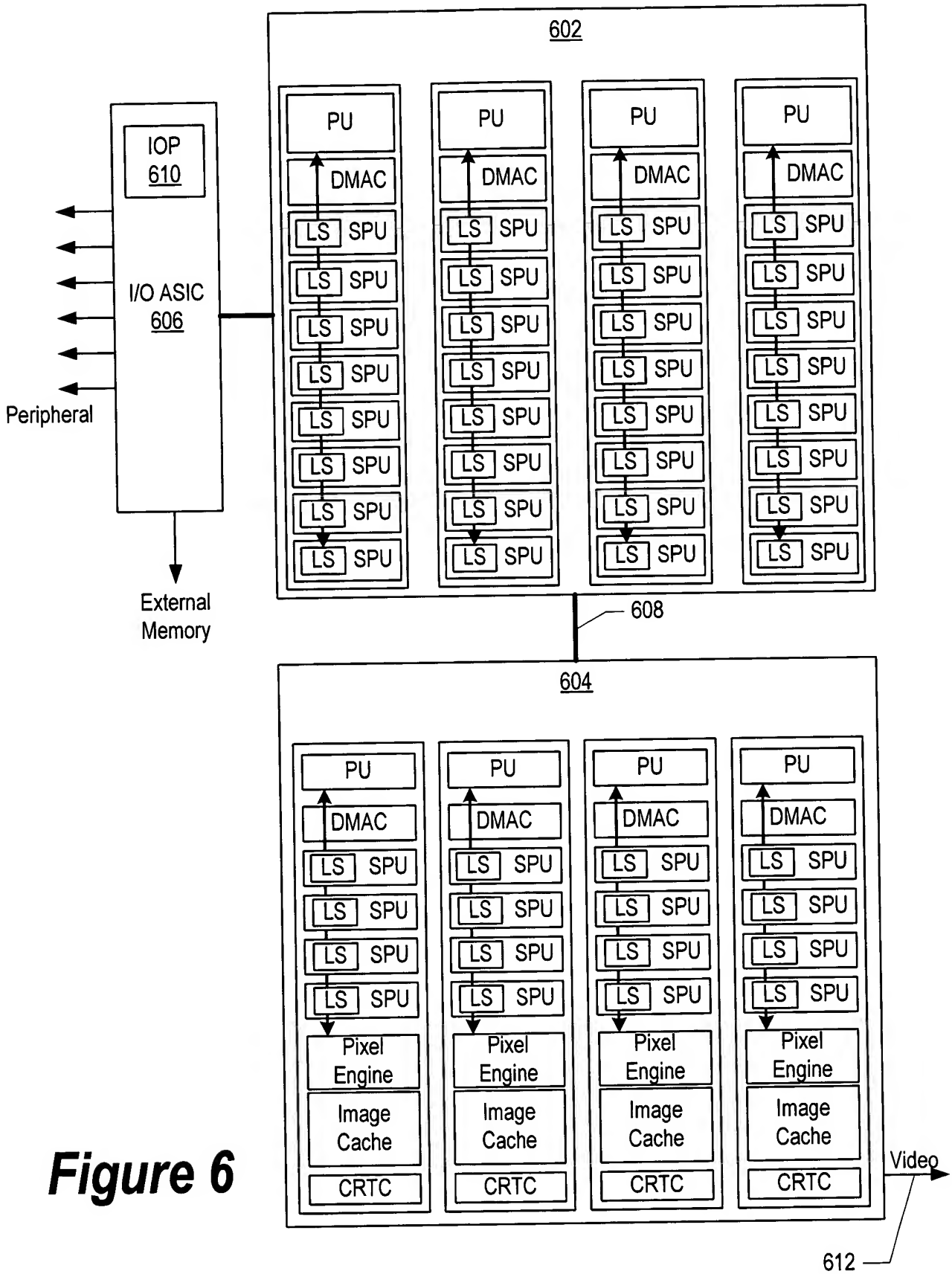
602
IOP
610
I/O ASIC
606
Peripheral
External
Memory
PU
DMAC
LS
SPU
608
604
Pixel
Engine
Image
Cache
CRTC
Video
612

Figure 6

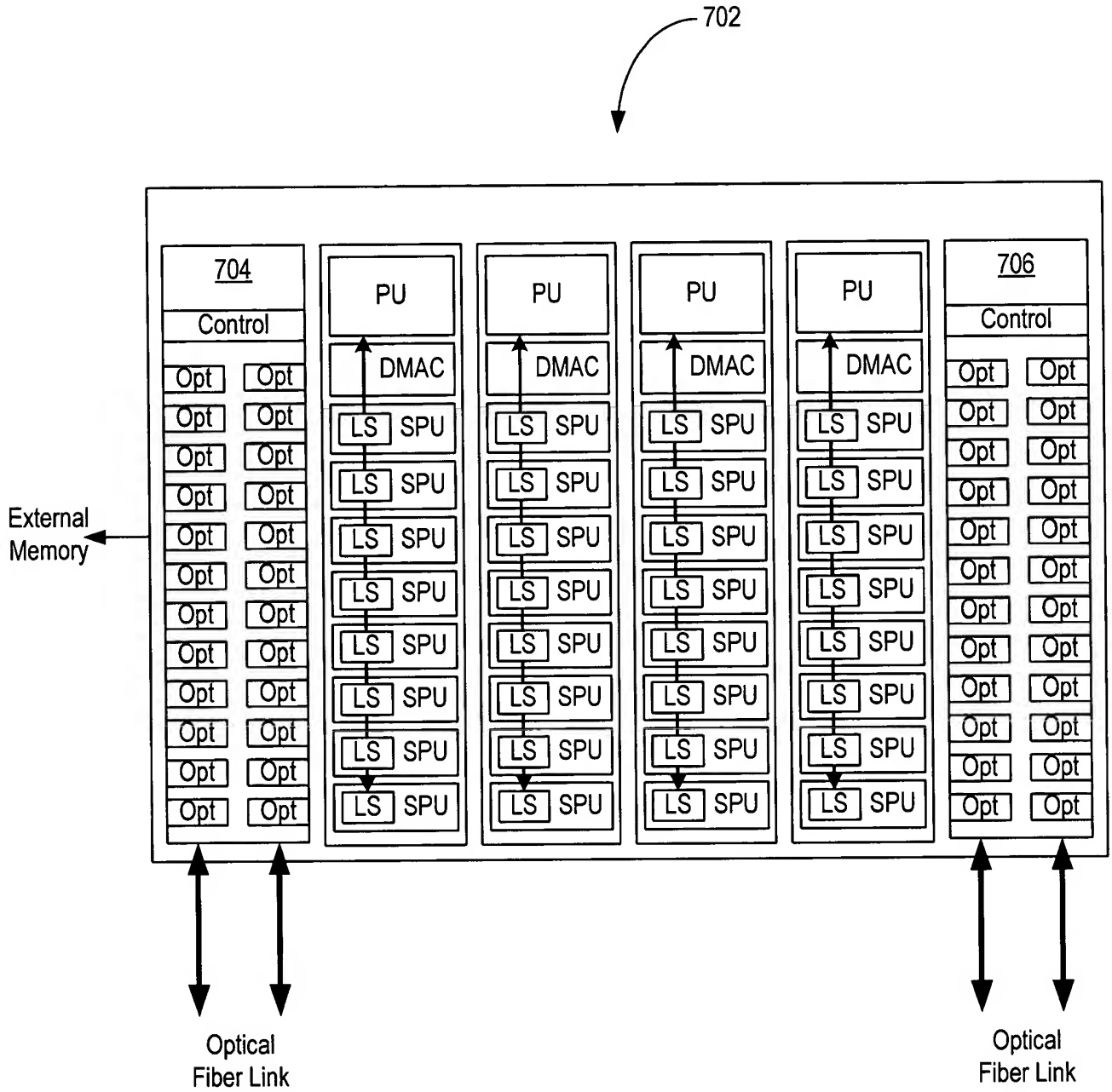
702
704
Control
Opt
706
Control
Opt
PU
DMAC
LS
SPU
External
Memory
Optical
Fiber Link
Optical
Fiber Link

Figure 7

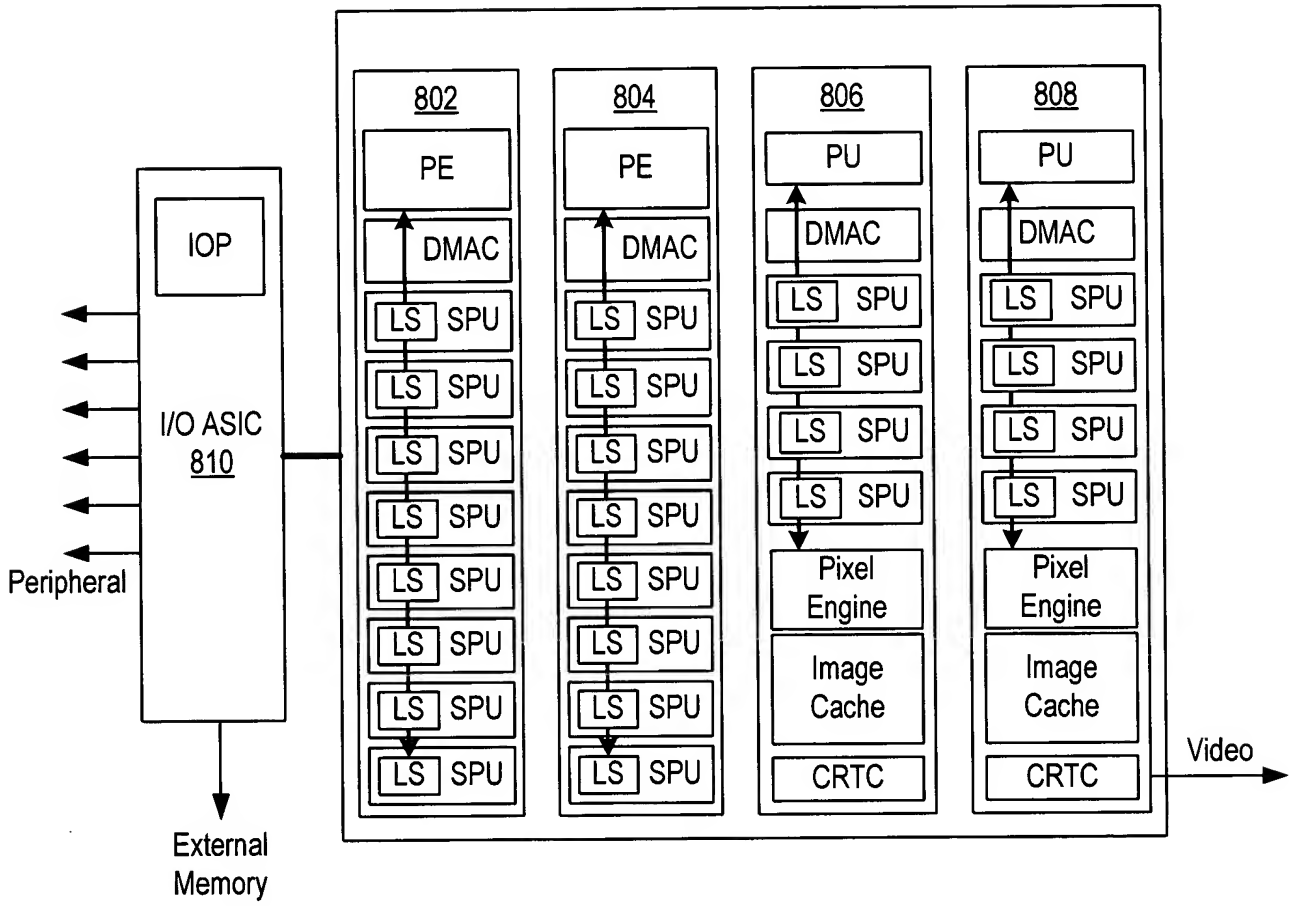
802
804
806
808
PE
PE
PU
PU
DMAC
DMAC
DMAC
DMAC
LS SPU
Pixel Engine
Image Cache
CRTC
IOP
I/O ASIC 810
Peripheral
External Memory
Video

Figure 8

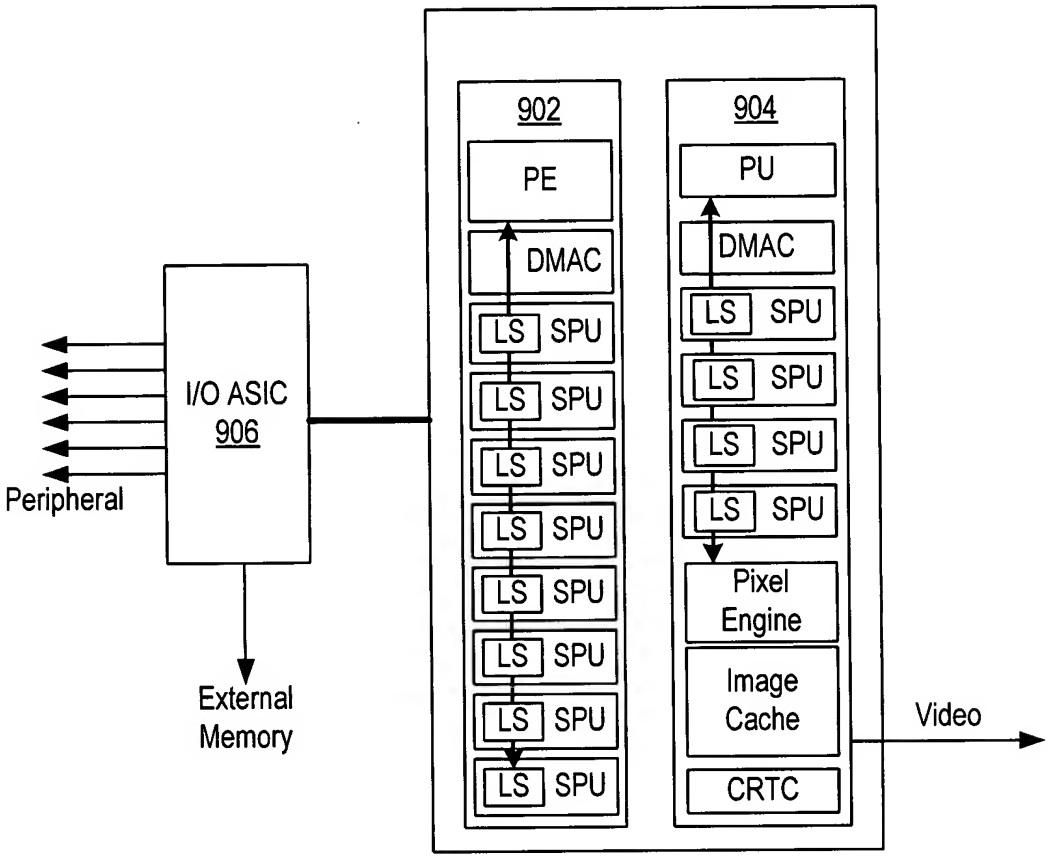
902
PE
DMAC
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
904
PU
DMAC
LS SPU
LS SPU
LS SPU
LS SPU
Pixel Engine
Image Cache
CRTC
Video
I/O ASIC 906
Peripheral
External Memory

Figure 9

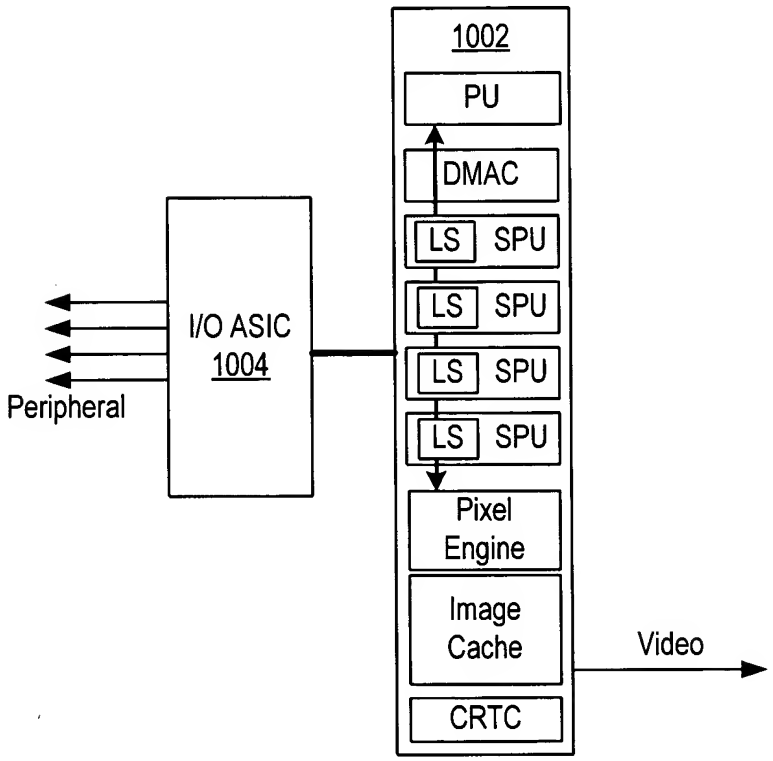
1002
PU
DMAC
LS
SPU
LS
SPU
LS
SPU
LS
SPU
Pixel Engine
Image Cache
CRTC
I/O ASIC
1004
Peripheral
Video

Figure 10

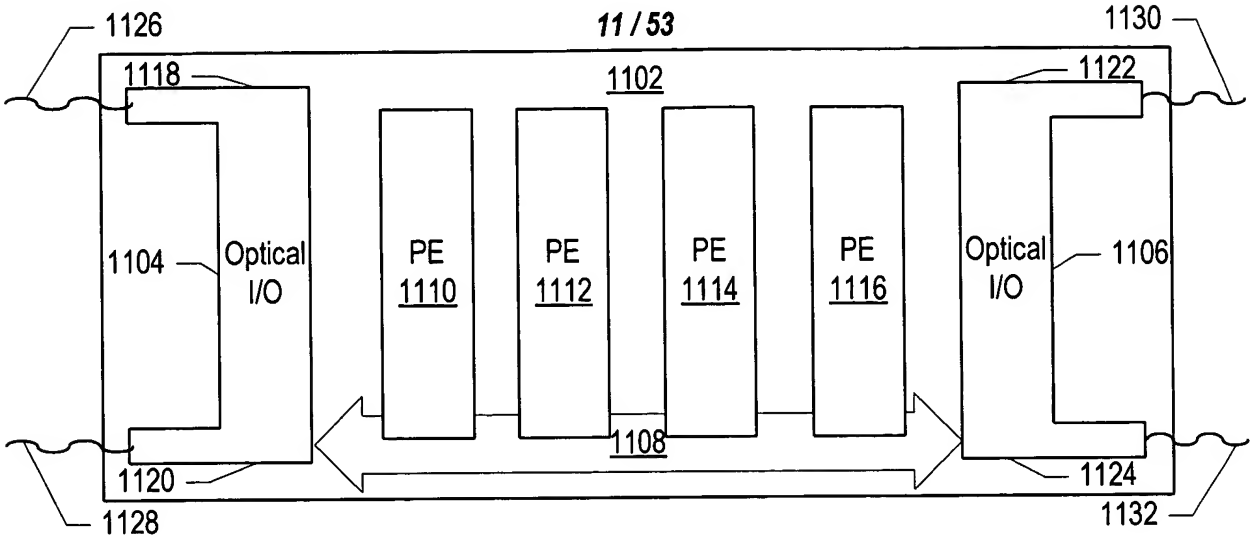

Figure 11A

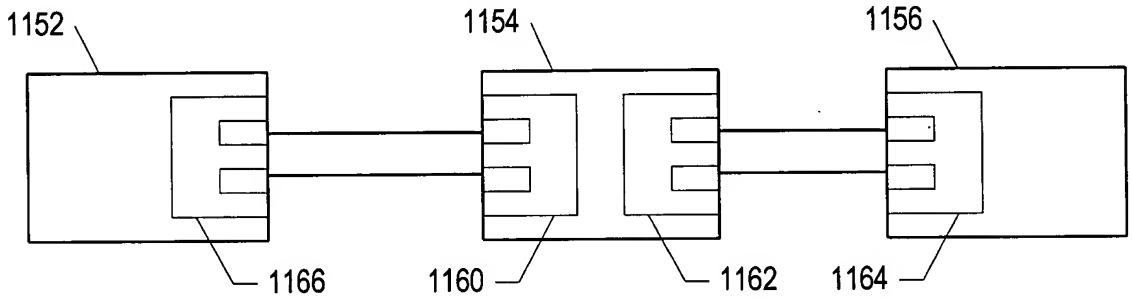

Figure 11B

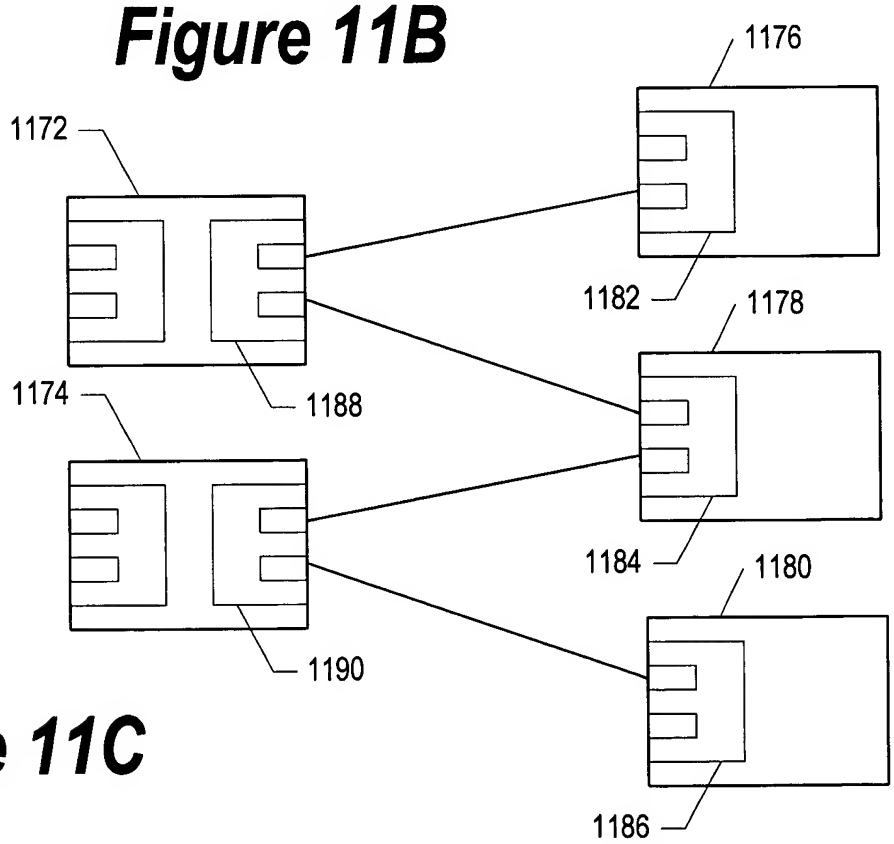

Figure 11C

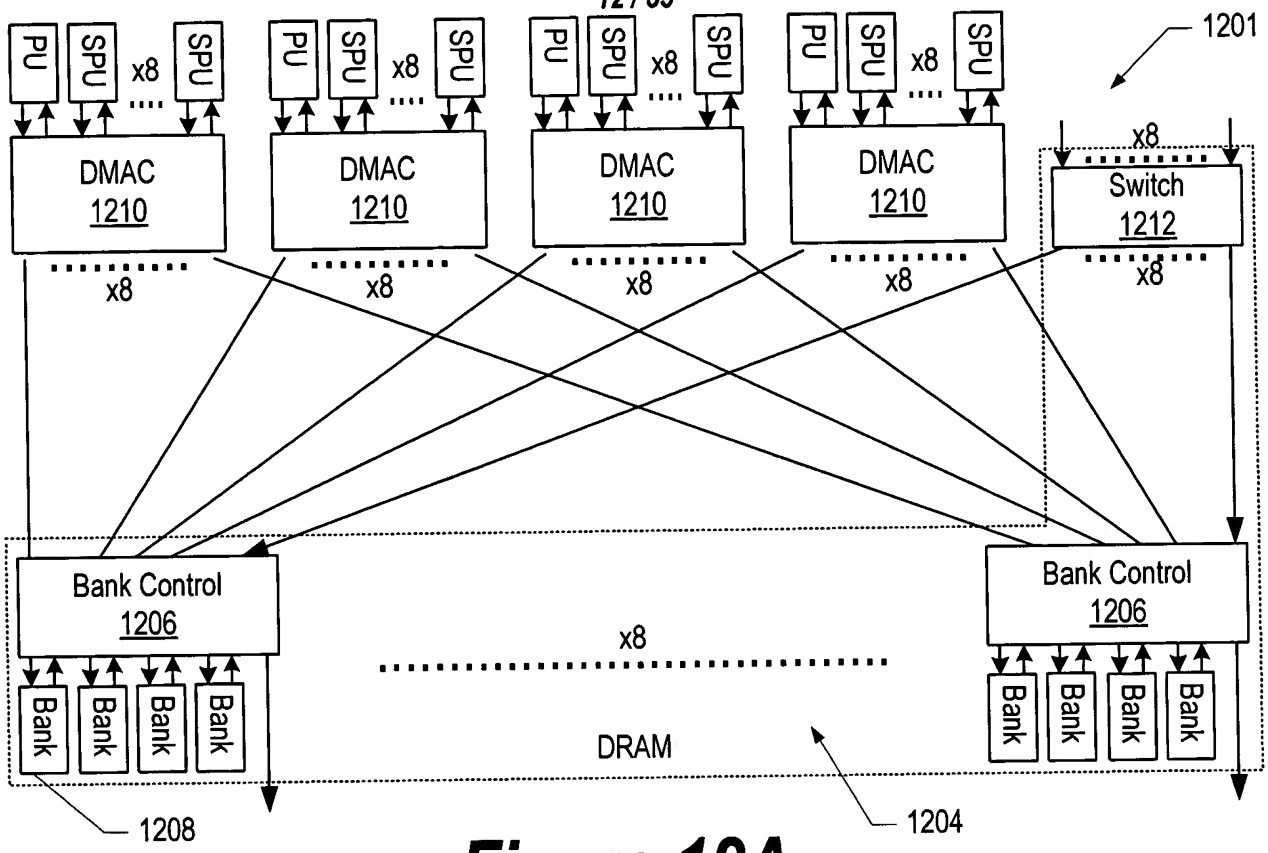

Figure 12A

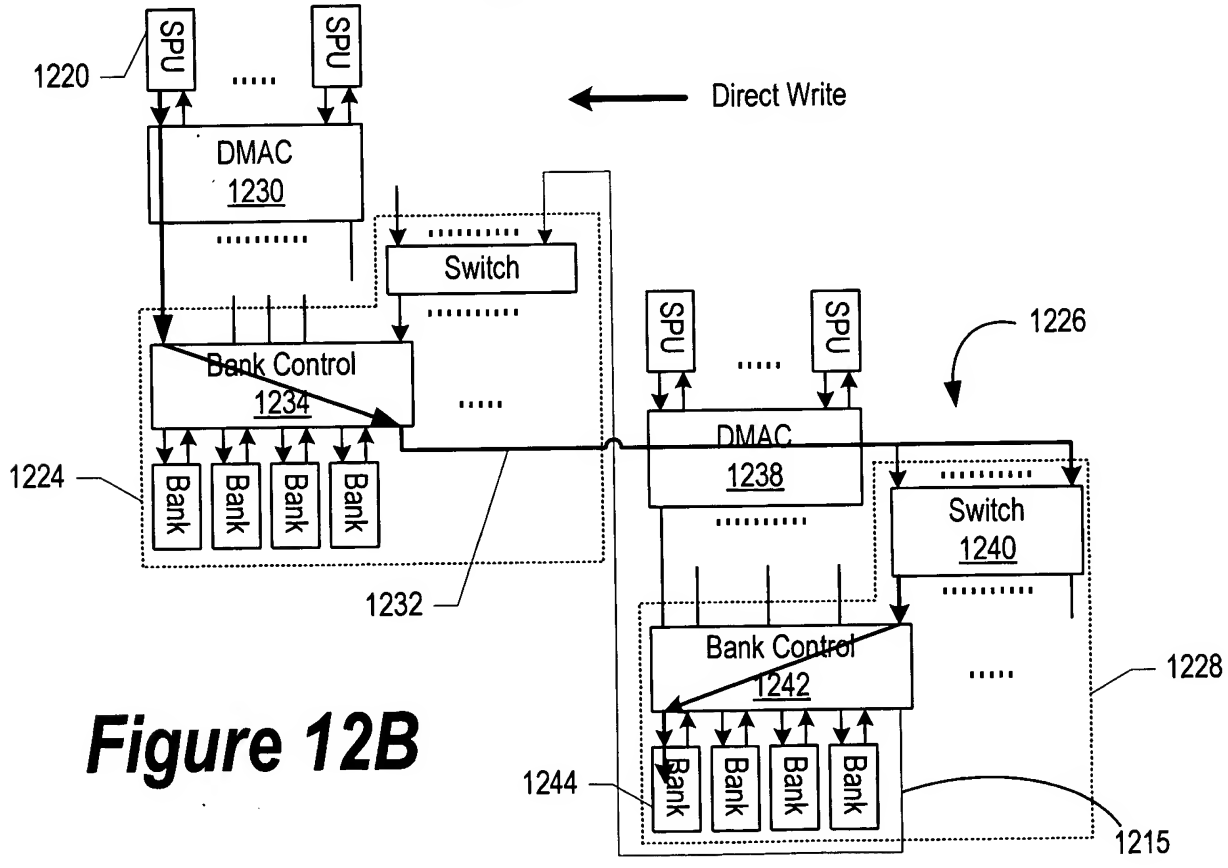

Figure 12B

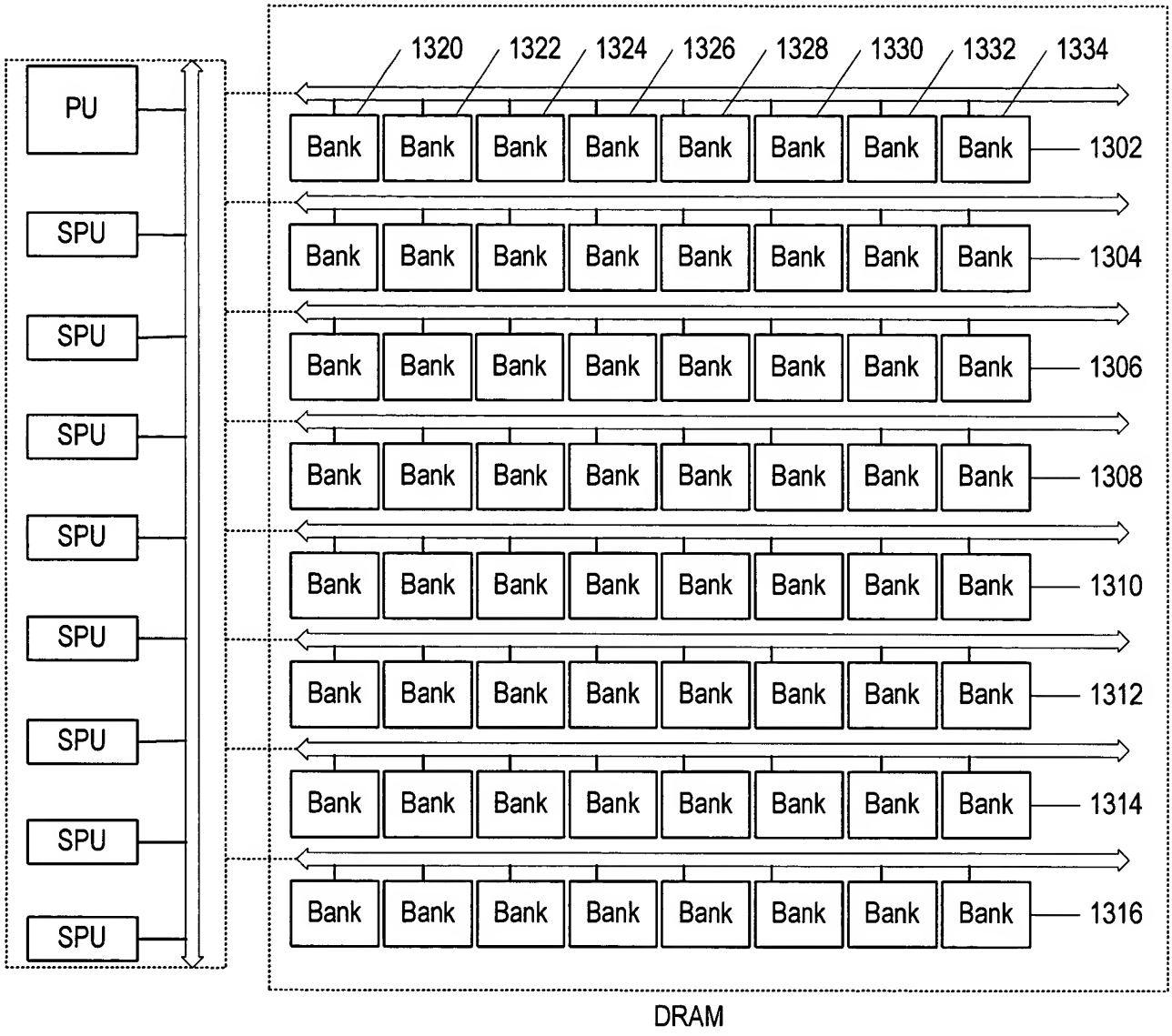
1320
1322
1324
1326
1328
1330
1332
1334
PU
SPU
SPU
SPU
SPU
SPU
SPU
SPU
SPU
Bank
1302
1304
1306
1308
1310
1312
1314
1316
DRAM

Figure 13

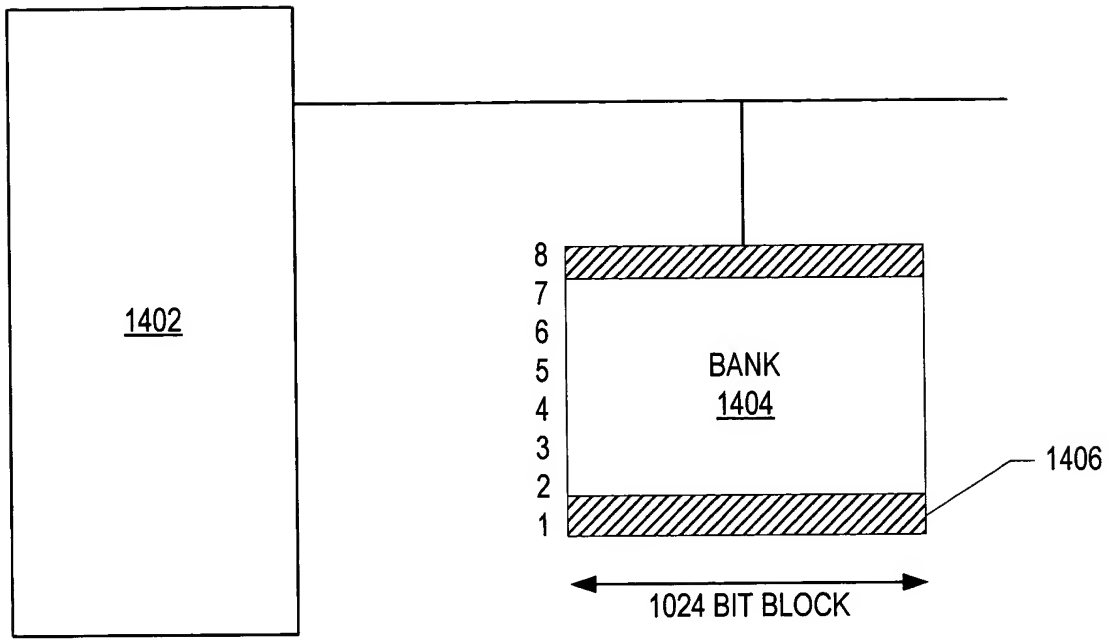

Figure 14A

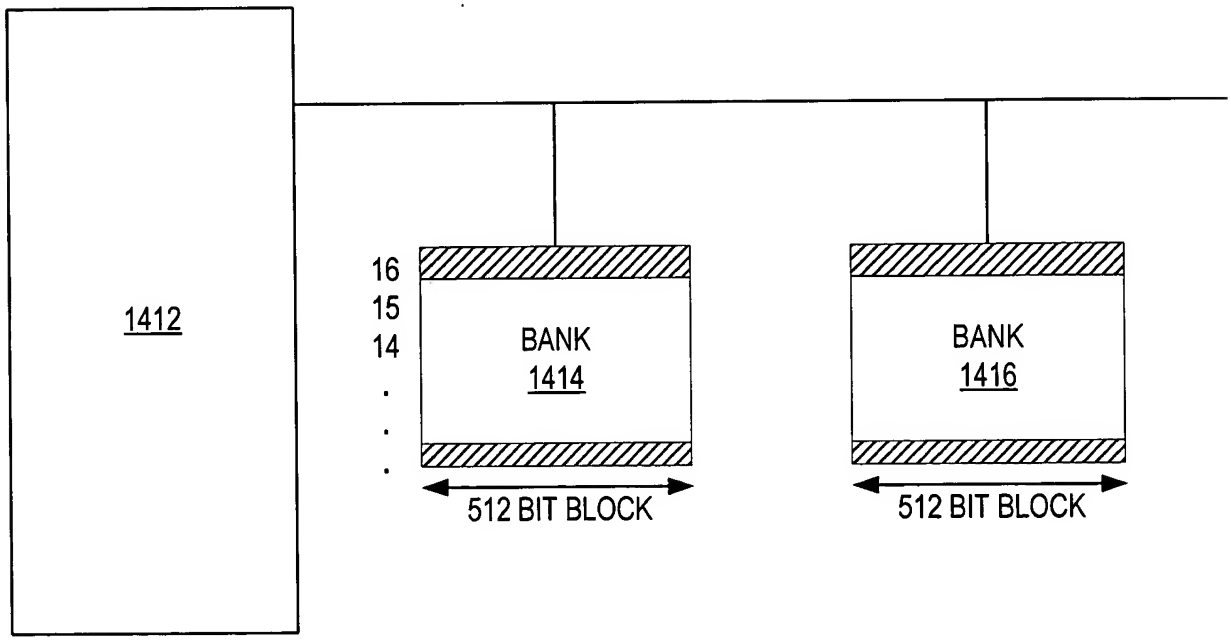

Figure 14B

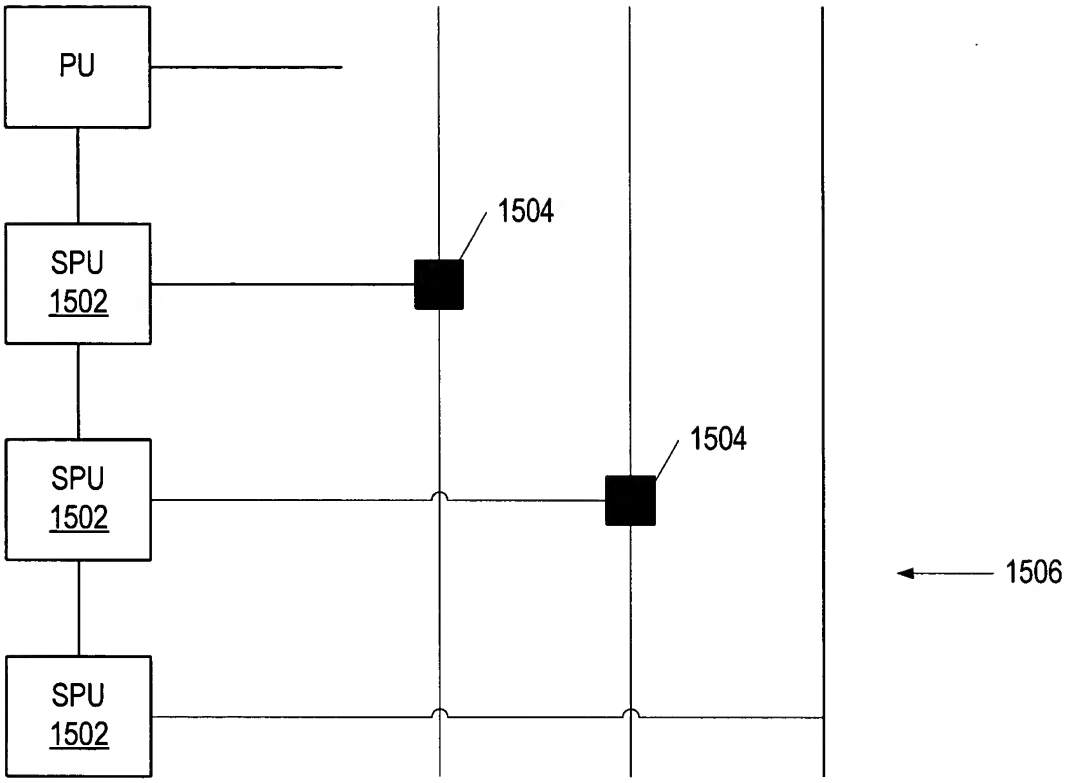

Figure 15

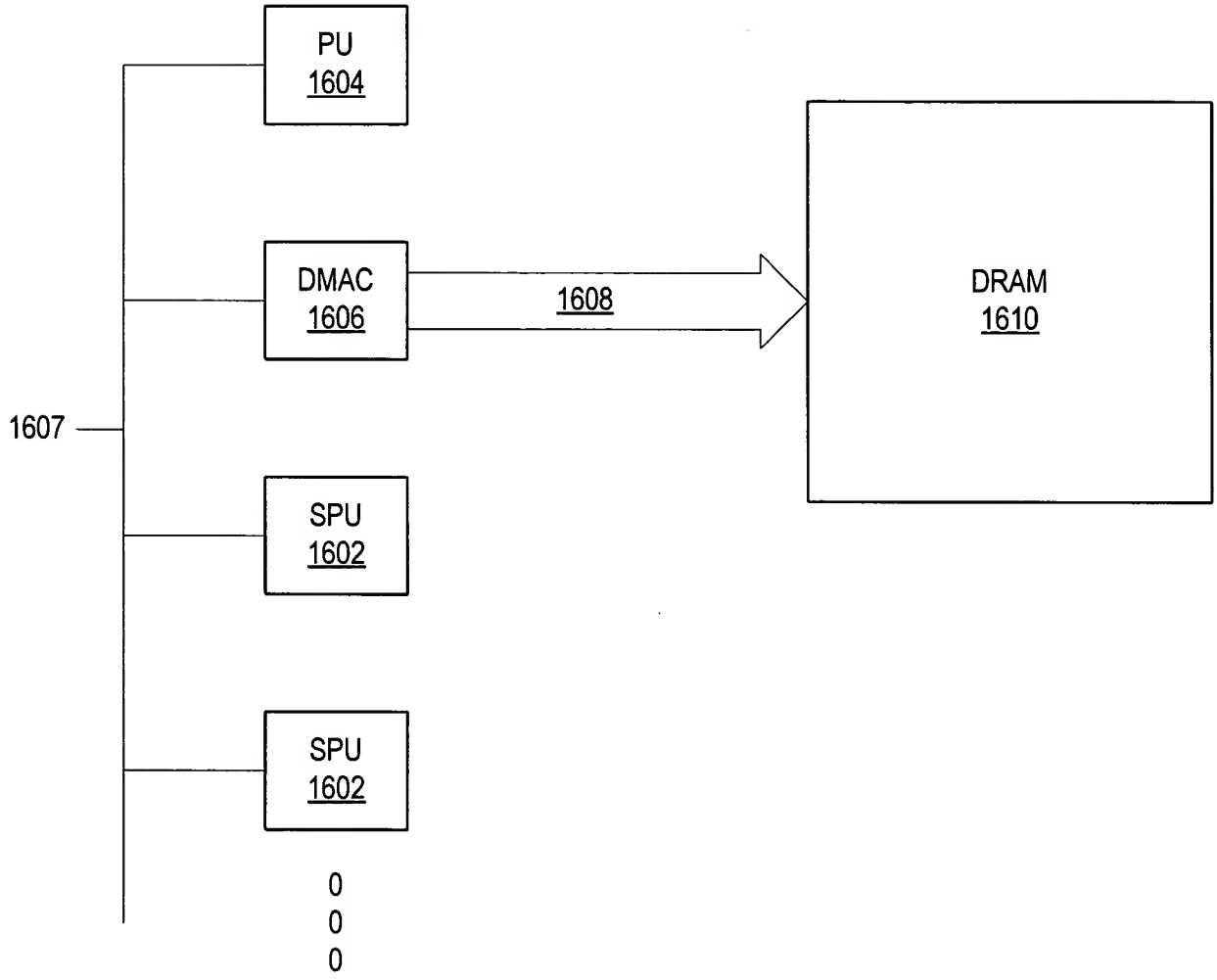

Figure 16

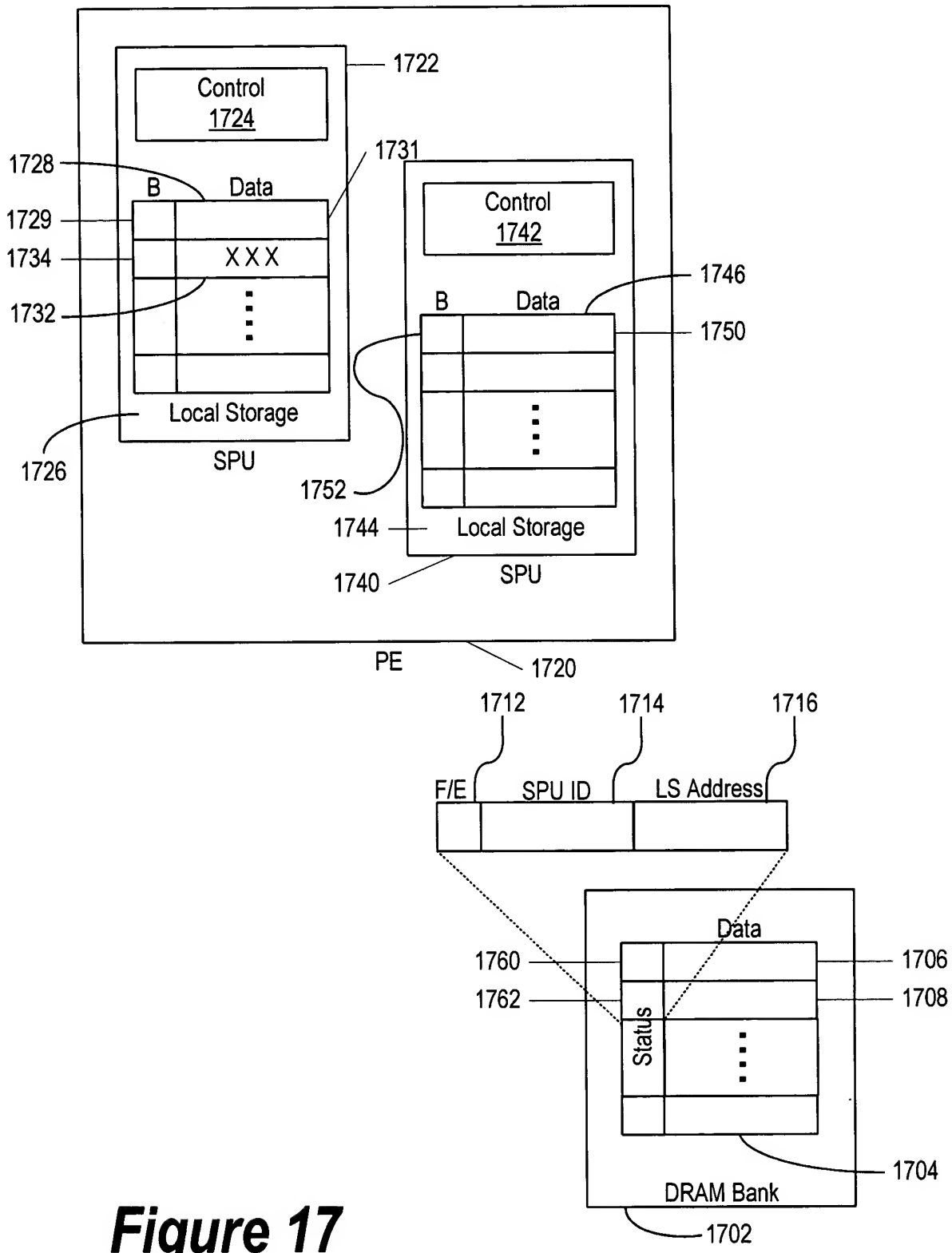
1722
Control
1724
1728
B
Data
1731
1729
1734
XXX
1732
Control
1742
1746
B
Data
1750
Local Storage
1726
SPU
1752
1744
Local Storage
1740
SPU
PE
1720
1712
1714
1716
F/E
SPU ID
LS Address
Data
1760
1762
1706
1708
Status
1704
DRAM Bank
1702

Figure 17

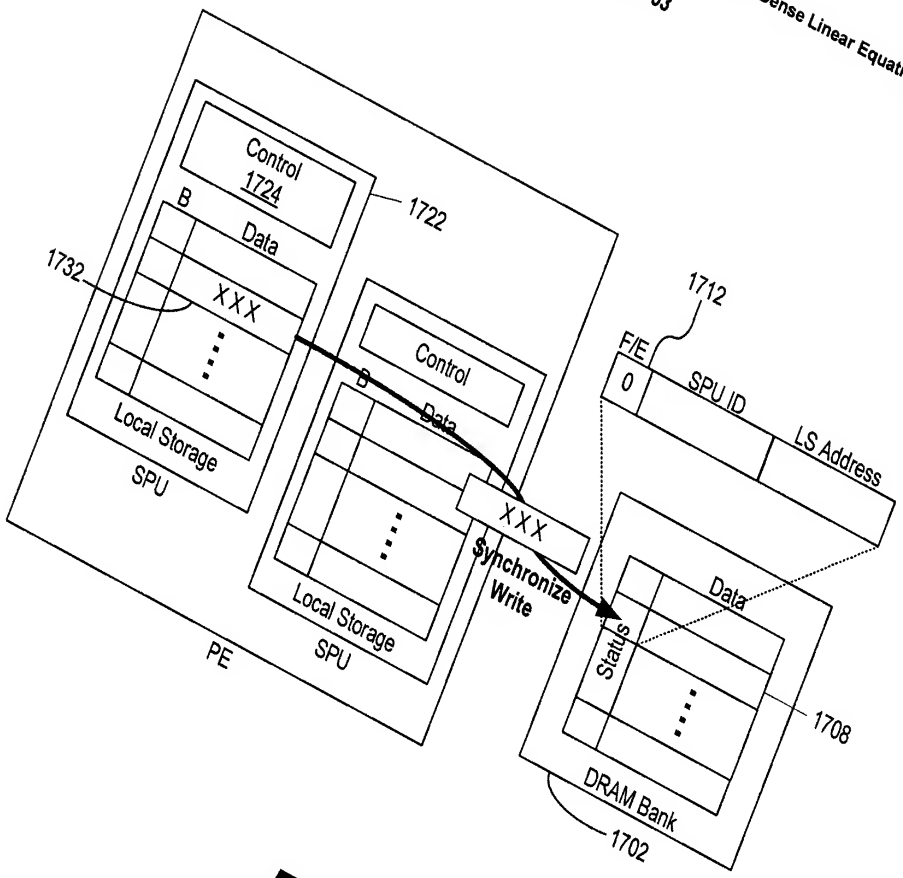
Control
1724
B
Data
XXX
1722
1732
Local Storage
SPU
Control
B
Data
XXX
Local Storage
SPU
PE
1712
F/E
0
SPU ID
LS Address
Synchronize
Write
Data
Status
1708
DRAM Bank
1702

Figure 18

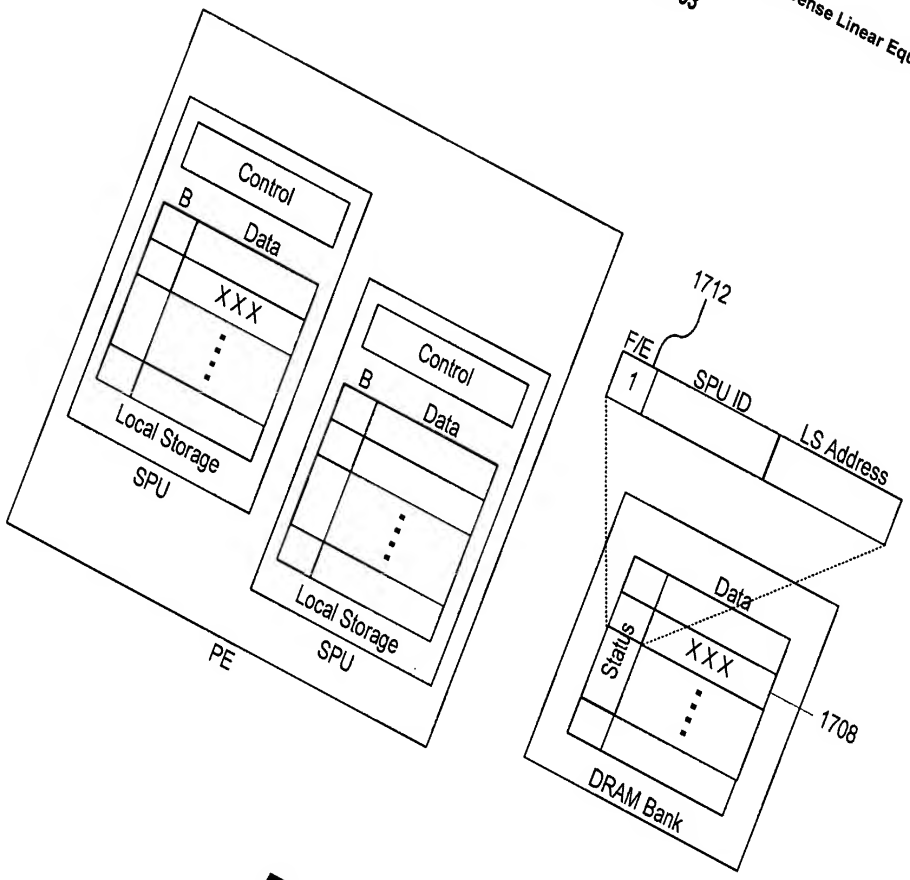
Control
B
Data
XXX
Local Storage
SPU
Control
B
Data
Local Storage
SPU
PE
1712
F/E
1
SPU ID
LS Address
Data
Status
XXX
1708
DRAM Bank

Figure 19

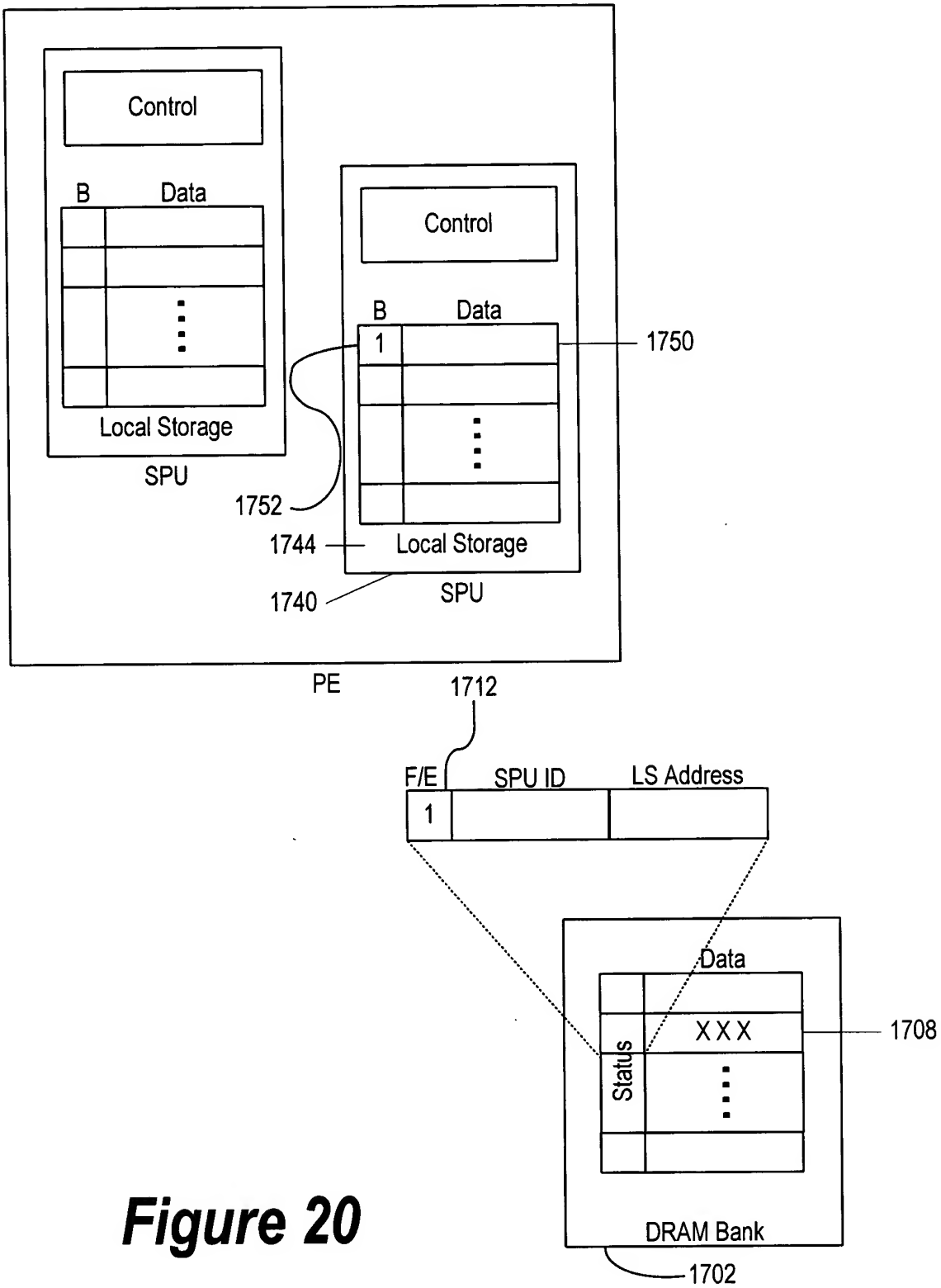
Control
B
Data
Local Storage
SPU
Control
B
Data
1
1750
1752
1744
Local Storage
1740
SPU
PE
1712
F/E
SPU ID
LS Address
1
Data
XXX
Status
1708
DRAM Bank
1702

Figure 20

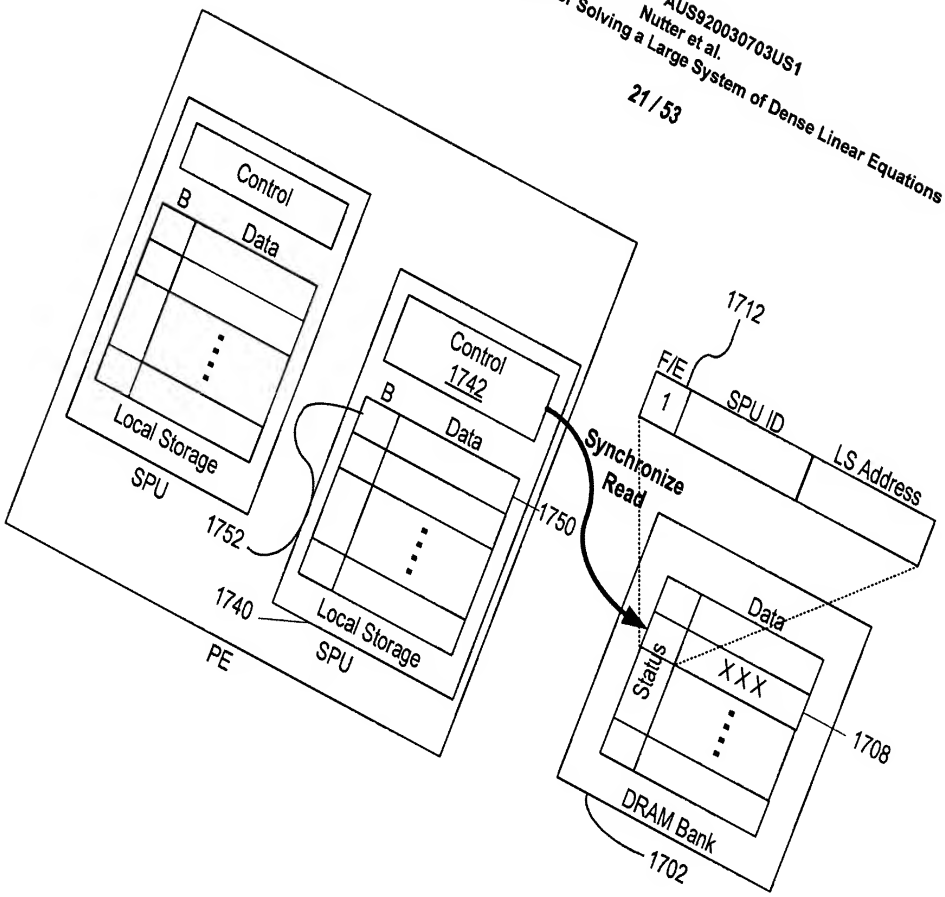
Control
B
Data
Local Storage
SPU
1752
Control
1742
B
Data
1750
Local Storage
SPU
1740
PE
1712
F/E
1
SPU ID
LS Address
Synchronize
Read
Data
Status
XXX
1708
DRAM Bank
1702

Figure 21

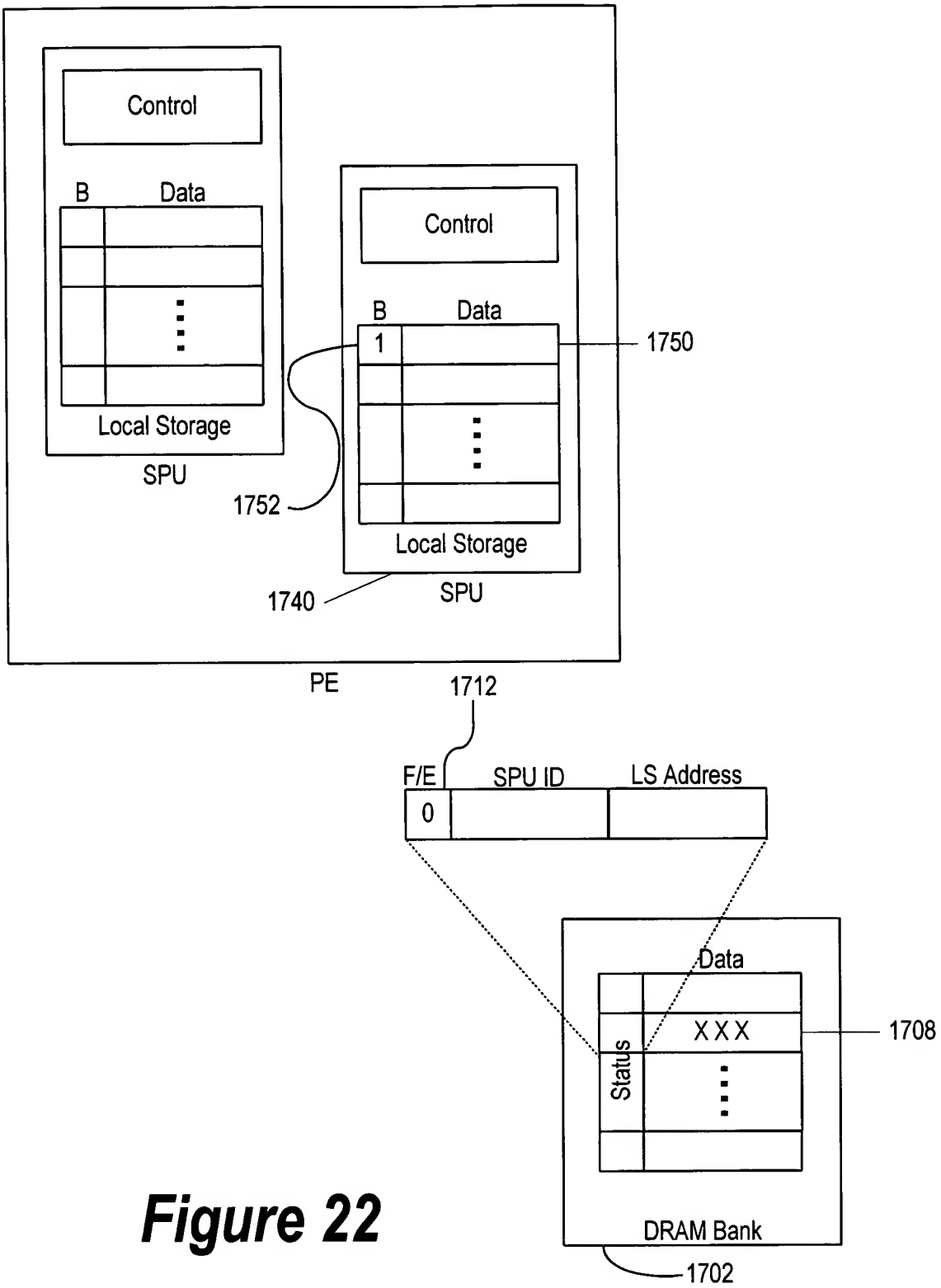
Control
B
Data
Local Storage
SPU
Control
B
Data
1
1750
1752
Local Storage
SPU
1740
PE
1712
F/E
SPU ID
LS Address
0
Data
XXX
Status
1708
DRAM Bank
1702

Figure 22

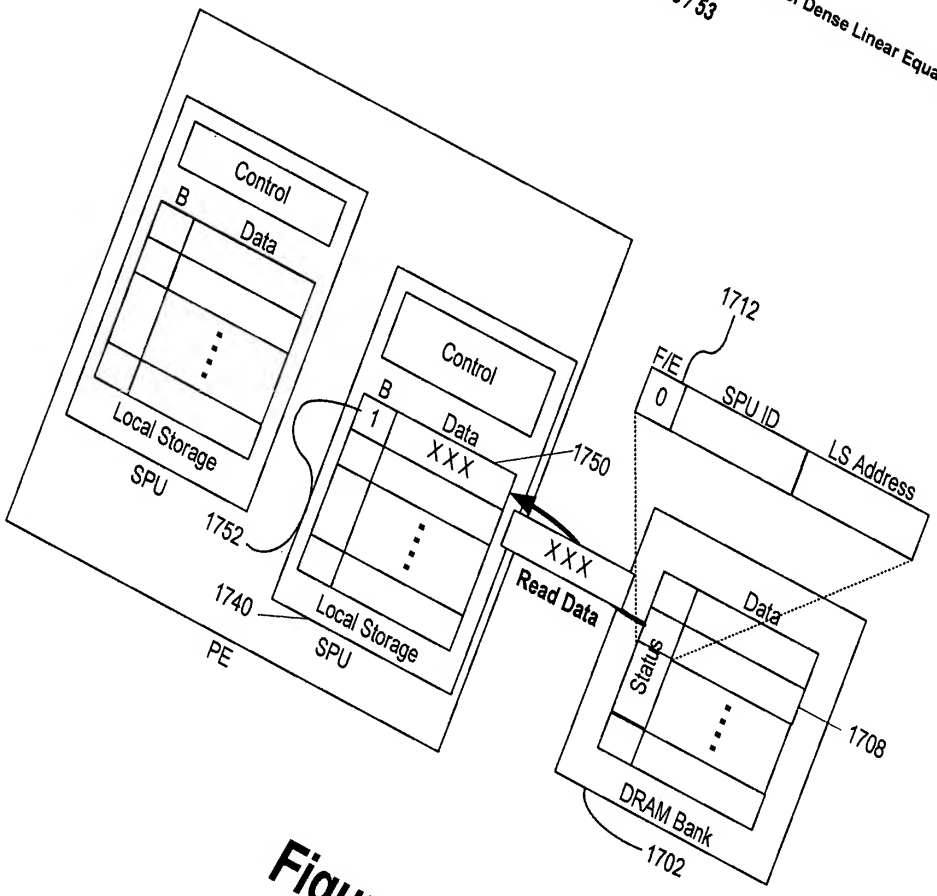
Control
B
Data
Local Storage
SPU
1752
Control
B
1
Data
XXX
1750
1740
Local Storage
SPU
PE
1712
F/E
0
SPU ID
LS Address
XXX
Read Data
Data
Status
1708
DRAM Bank
1702

Figure 23

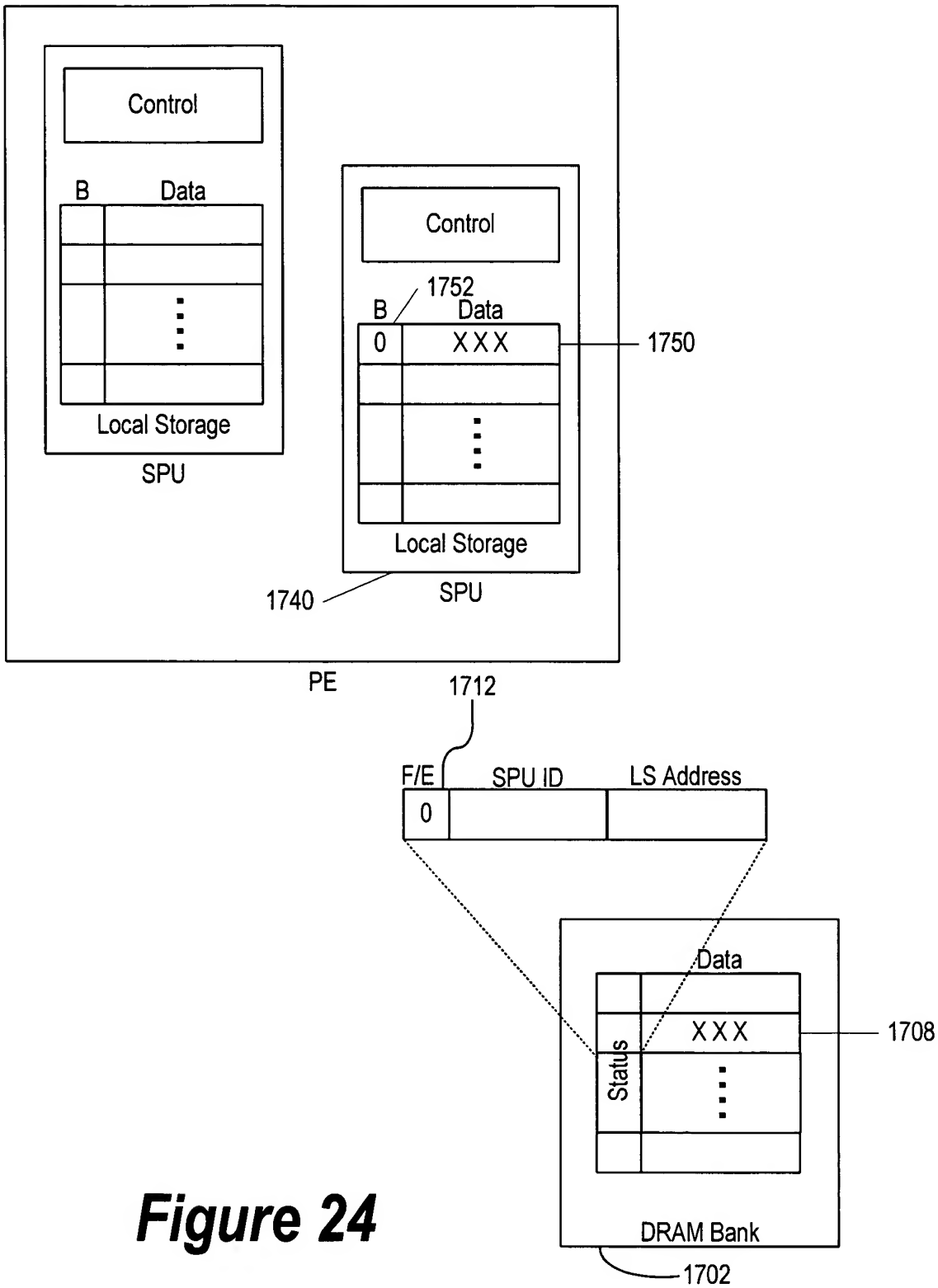
Control
B
Data
Local Storage
SPU
Control
1752
B
Data
0
XXX
1750
Local Storage
SPU
1740
PE
1712
F/E
SPU ID
LS Address
0
Data
XXX
1708
Status
DRAM Bank
1702

Figure 24

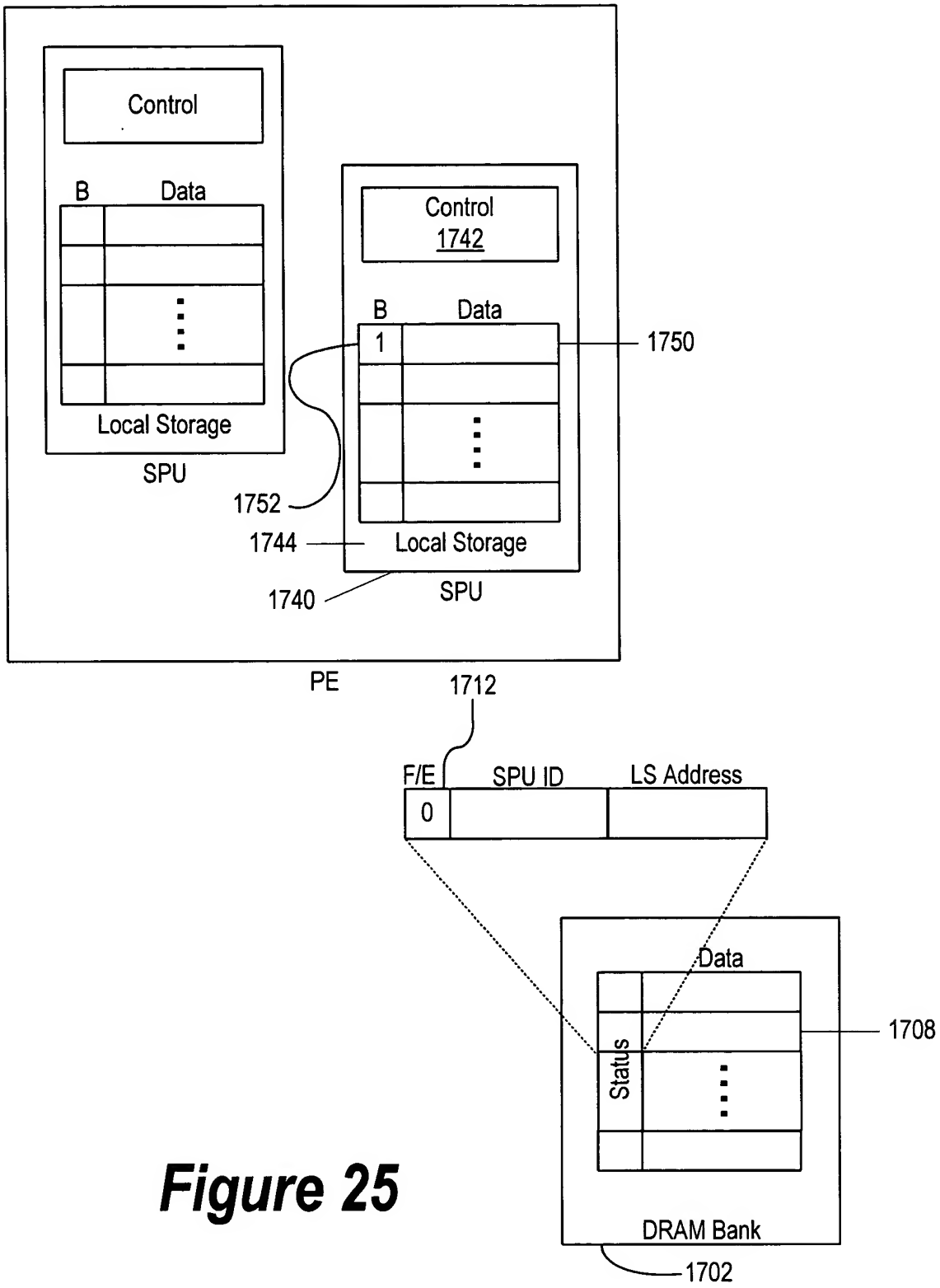
Control
B
Data
Local Storage
SPU
Control
1742
B
Data
1
1750
1752
1744
Local Storage
1740
SPU
PE
1712
F/E
SPU ID
LS Address
0
Data
Status
1708
DRAM Bank
1702

Figure 25

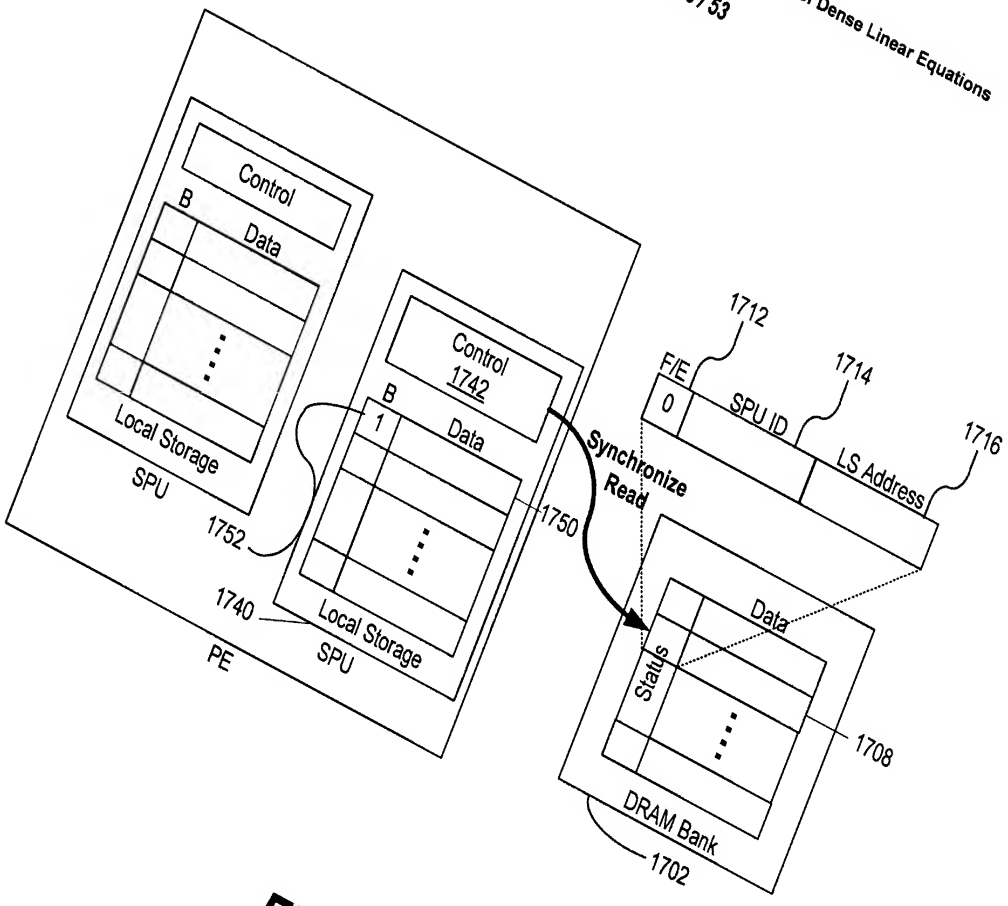
Control
B
Data
Local Storage
SPU
1752
Control
1742
B
1
Data
1750
1740
Local Storage
SPU
PE
1712
F/E
0
1714
SPU ID
1716
LS Address
Synchronize
Read
Data
Status
1708
DRAM Bank
1702

Figure 26

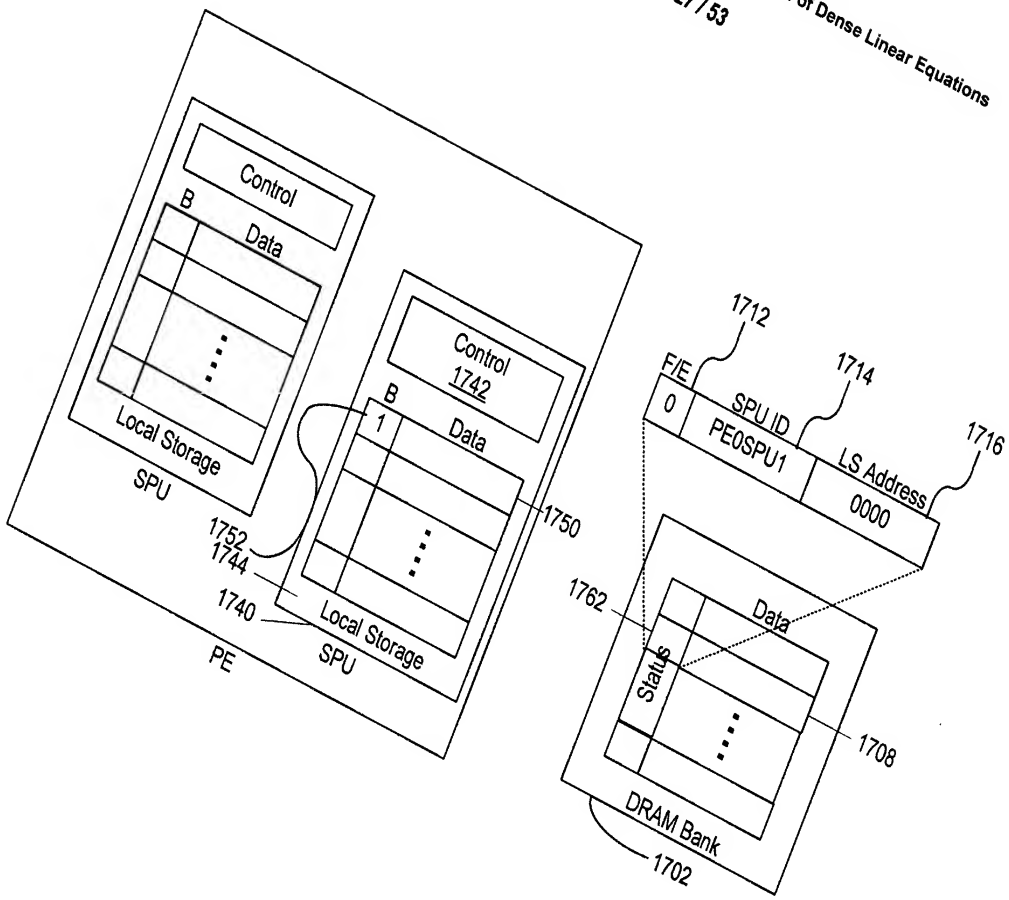
Control
B
Data
Local Storage
SPU
Control
1742
B
1
Data
1750
1752
1744
1740
Local Storage
SPU
PE
1712
F/E
0
1714
SPU ID
PE0SPU1
LS Address
0000
1716
1762
Data
Status
1708
DRAM Bank
1702

Figure 27

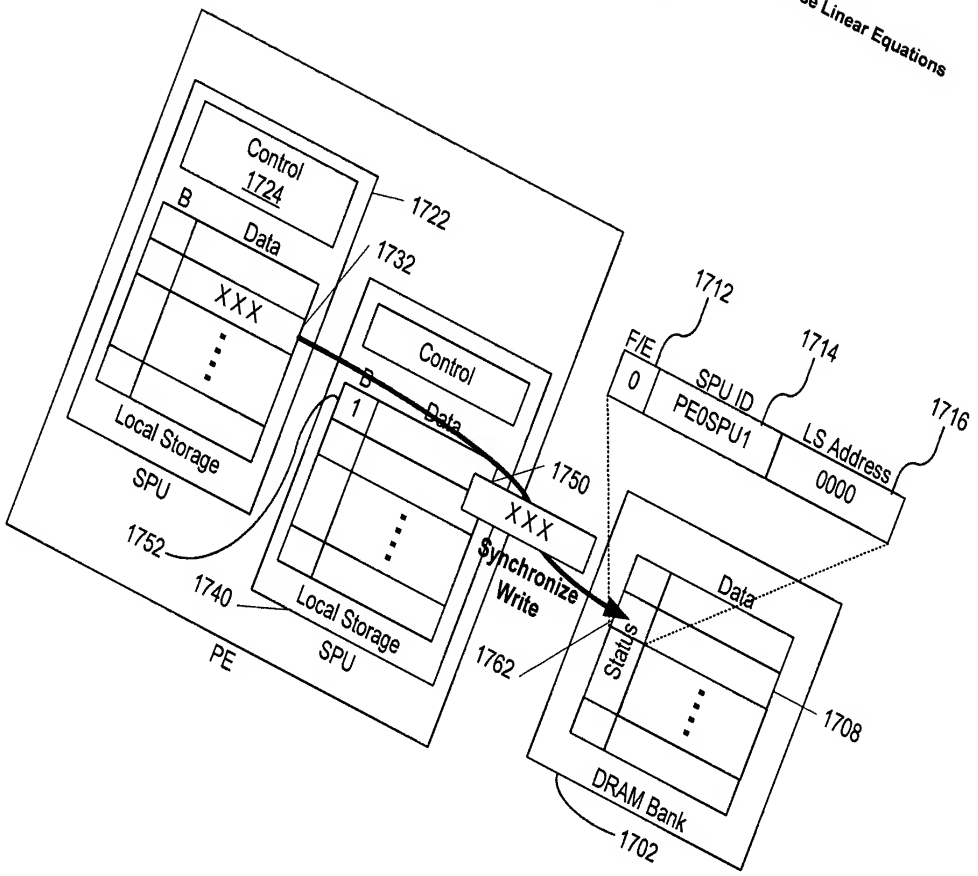
Control
1724
B
Data
XXX
1722
1732
Local Storage
SPU
1752
1740
Control
B
1
Data
Local Storage
SPU
PE
1750
XXX
Synchronize
Write
1762
1712
F/E
0
SPU ID
PE0SPU1
1714
LS Address
0000
1716
Data
Status
1708
DRAM Bank
1702

Figure 28

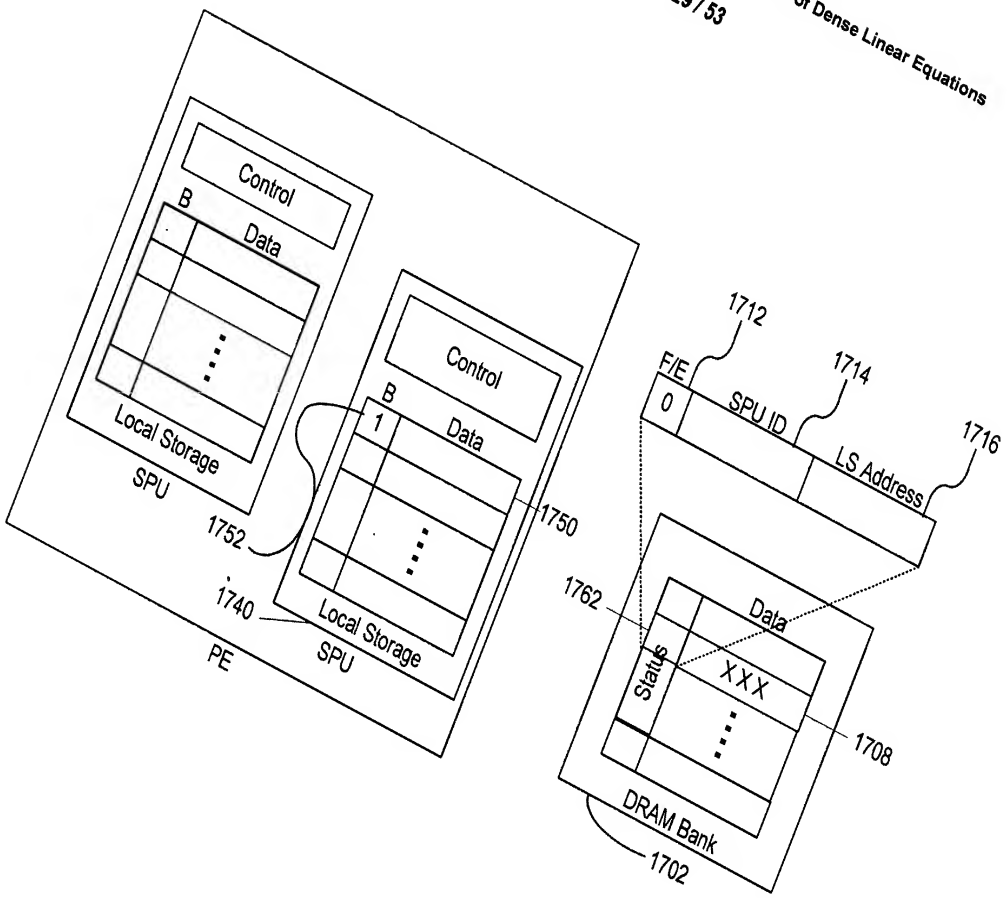
Control
B
Data
Local Storage
SPU
1752
Control
B
1
Data
1750
1740
Local Storage
SPU
PE
1712
F/E
0
1714
SPU ID
1716
LS Address
1762
Data
Status
XXX
1708
DRAM Bank
1702

Figure 29

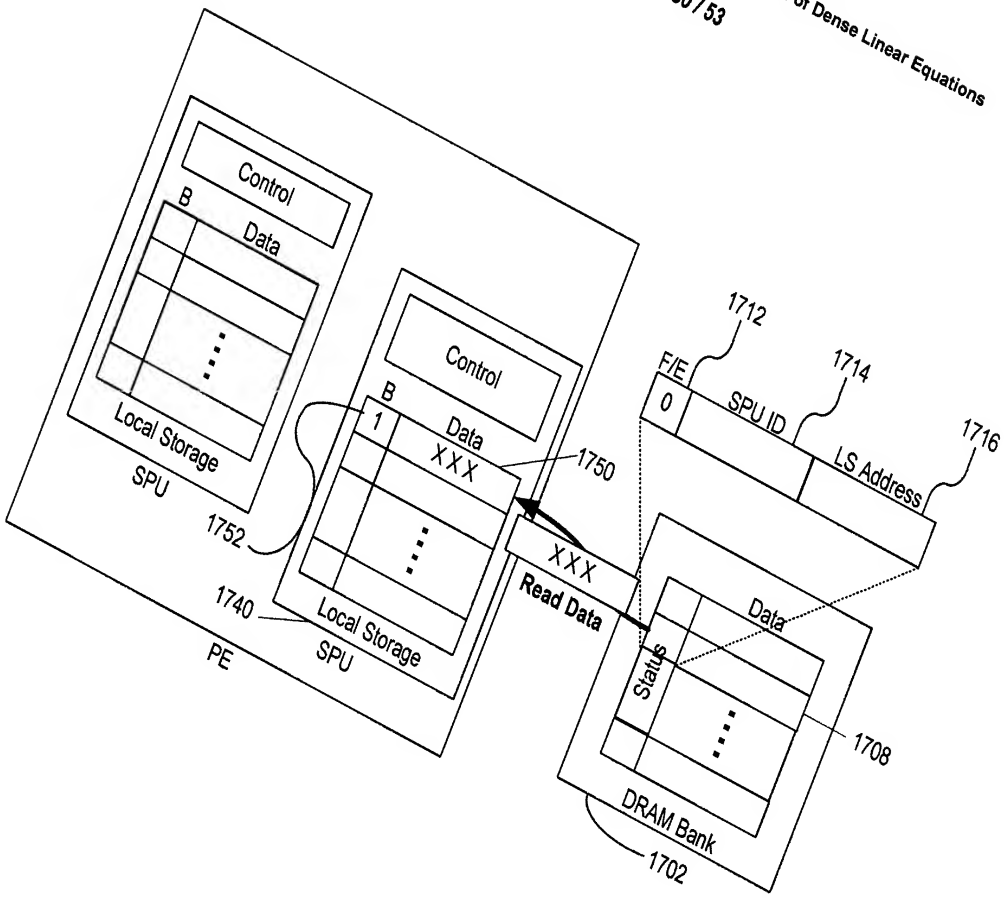
Control
B
Data
Local Storage
SPU
1752
Control
B
1
Data
XXX
1750
Local Storage
SPU
1740
PE
1712
F/E
0
1714
SPU ID
1716
LS Address
XXX
Read Data
Data
Status
1708
DRAM Bank
1702

Figure 30

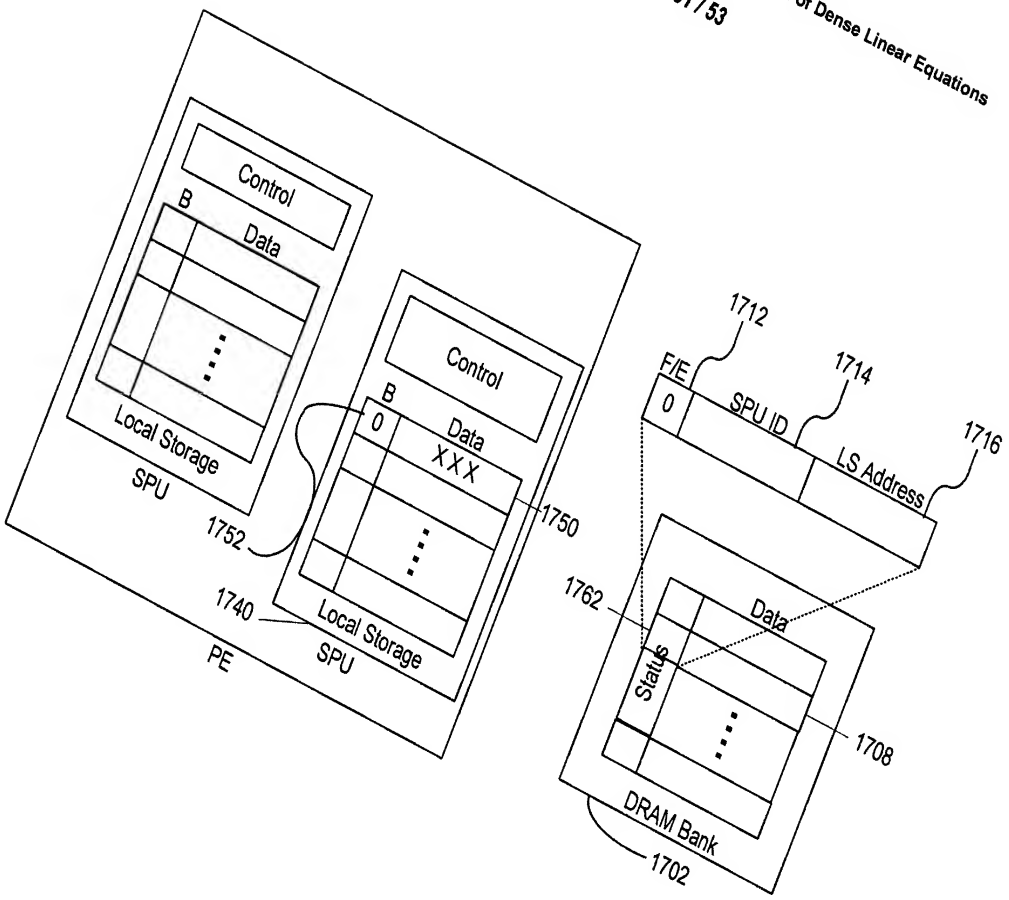
Control
B
Data
Local Storage
SPU
1752
Control
B
0
Data
XXX
1750
Local Storage
SPU
1740
PE
1712
F/E
1714
0
SPU ID
1716
LS Address
1762
Data
Status
1708
DRAM Bank
1702

Figure 31

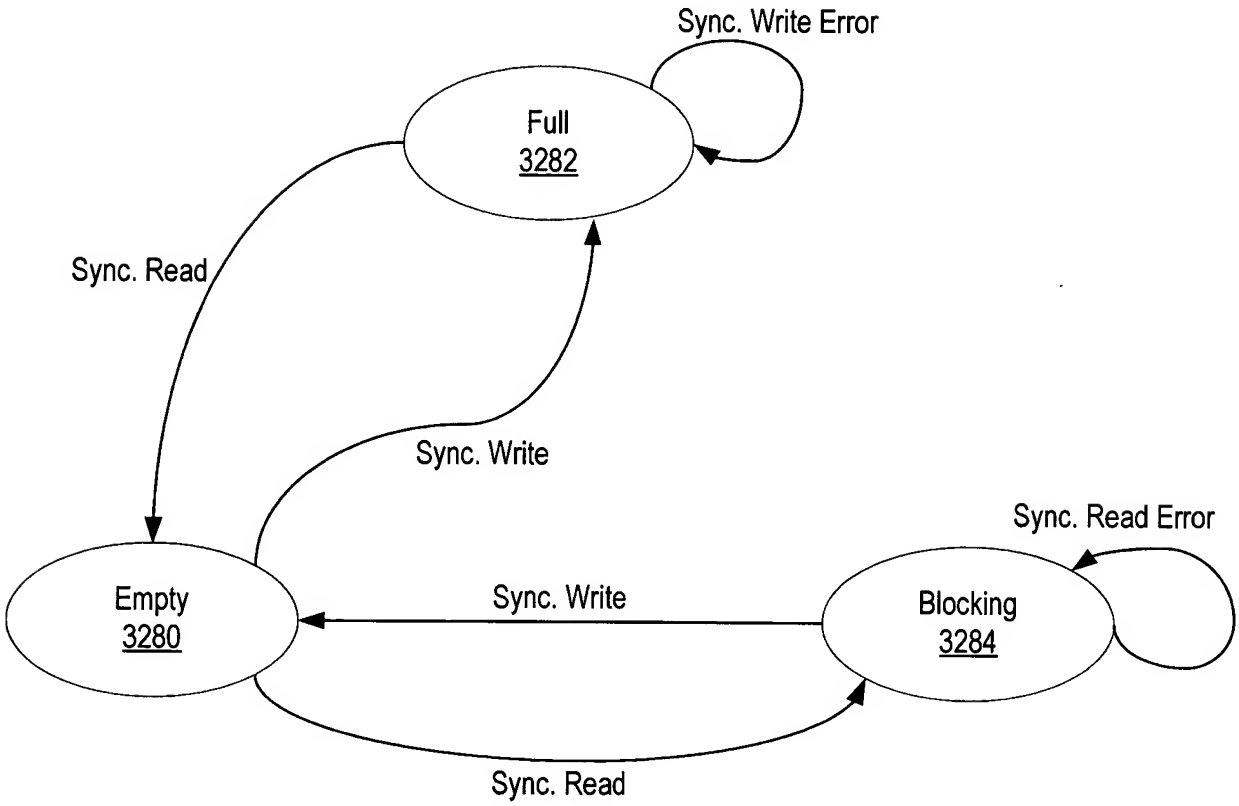
Sync. Write Error
Full
3282
Sync. Read
Sync. Write
Sync. Read Error
Empty
3280
Sync. Write
Blocking
3284
Sync. Read

Figure 32

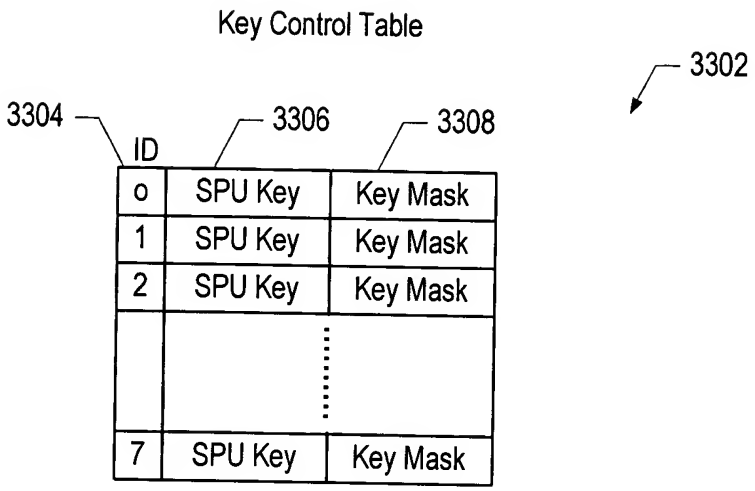
Key Control Table
3302
3304
ID
3306
SPU Key
3308
Key Mask
0
1
2
7

Figure 33

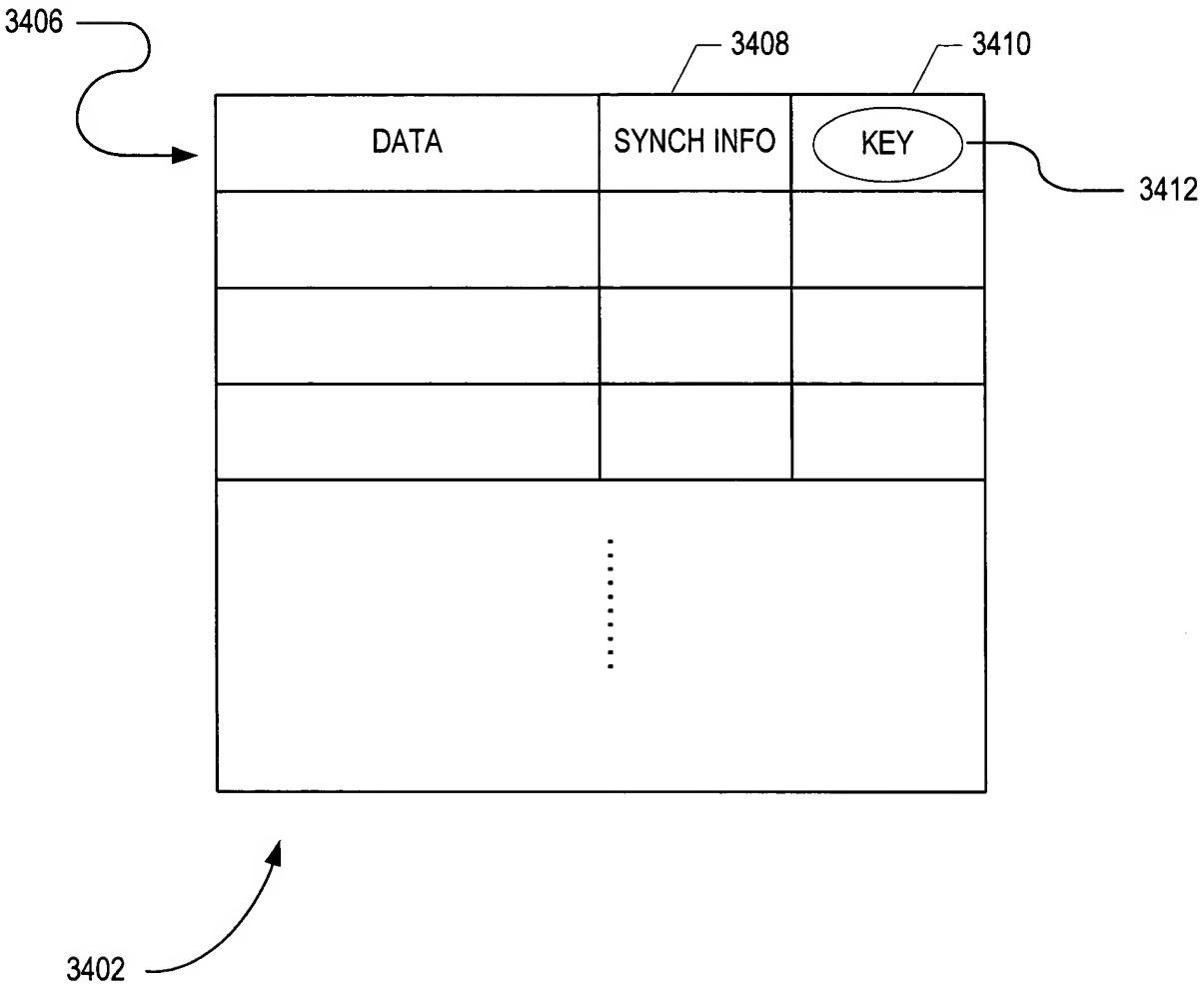

Figure 34

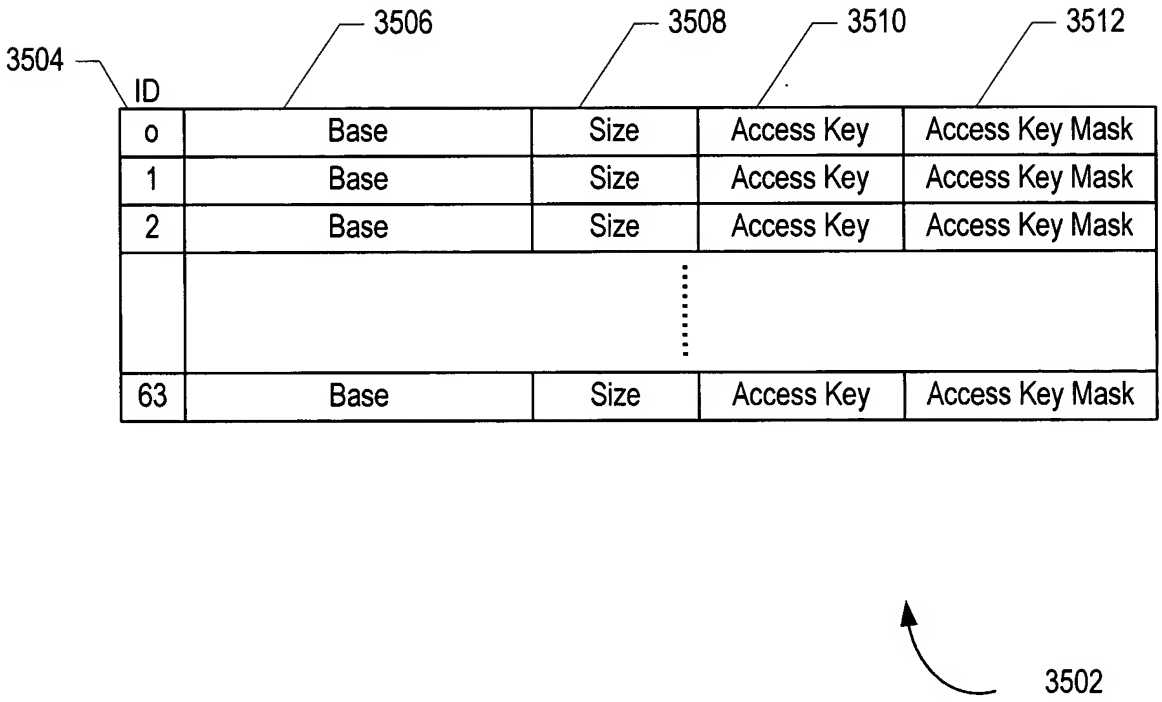
Memory Access Control Table
3504
ID
3506
3508
3510
3512
0
Base
Size
Access Key
Access Key Mask
1
Base
Size
Access Key
Access Key Mask
2
Base
Size
Access Key
Access Key Mask
63
Base
Size
Access Key
Access Key Mask
3502

Figure 35

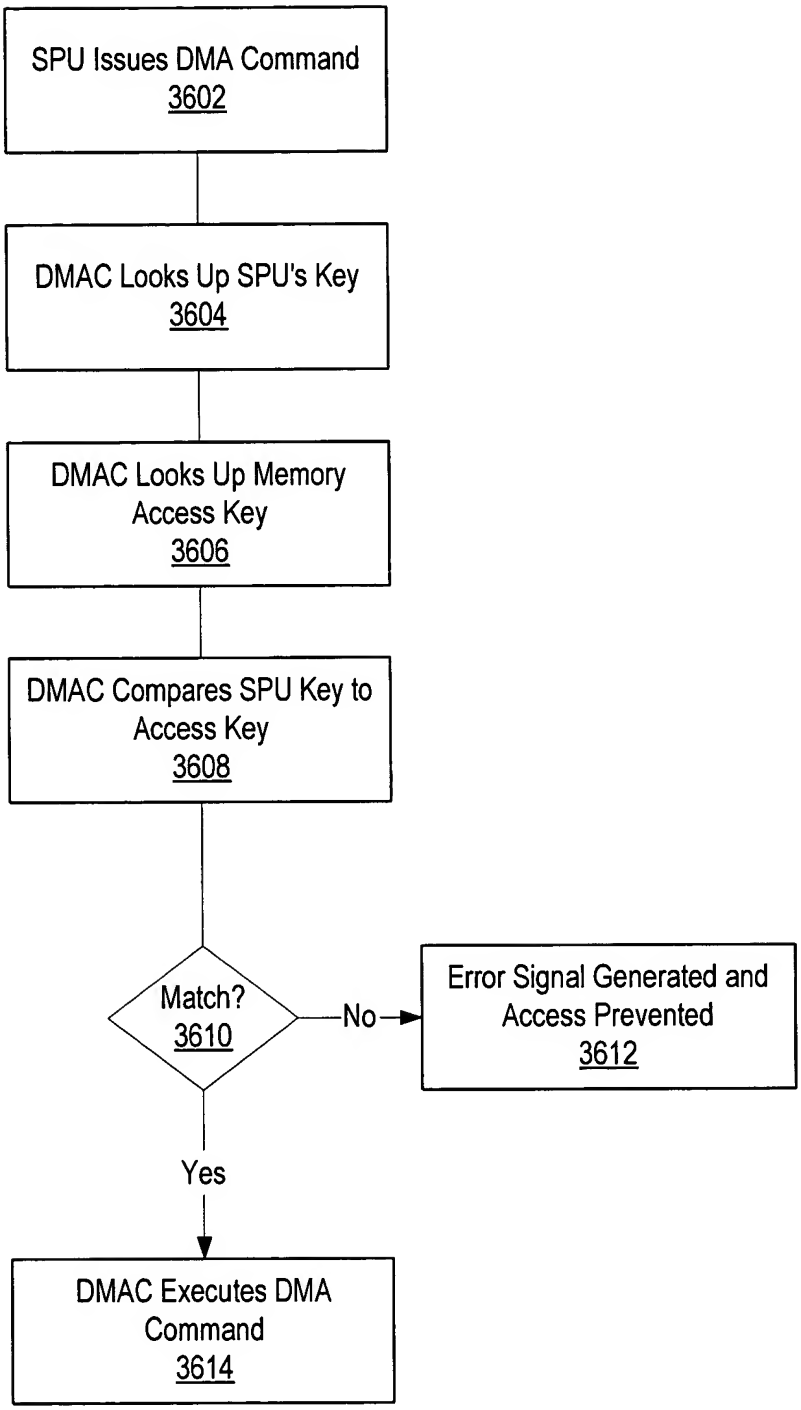
SPU Issues DMA Command
3602
DMAC Looks Up SPU's Key
3604
DMAC Looks Up Memory Access Key
3606
DMAC Compares SPU Key to Access Key
3608
Match?
3610
No
Error Signal Generated and Access Prevented
3612
Yes
DMAC Executes DMA Command
3614

Figure 36

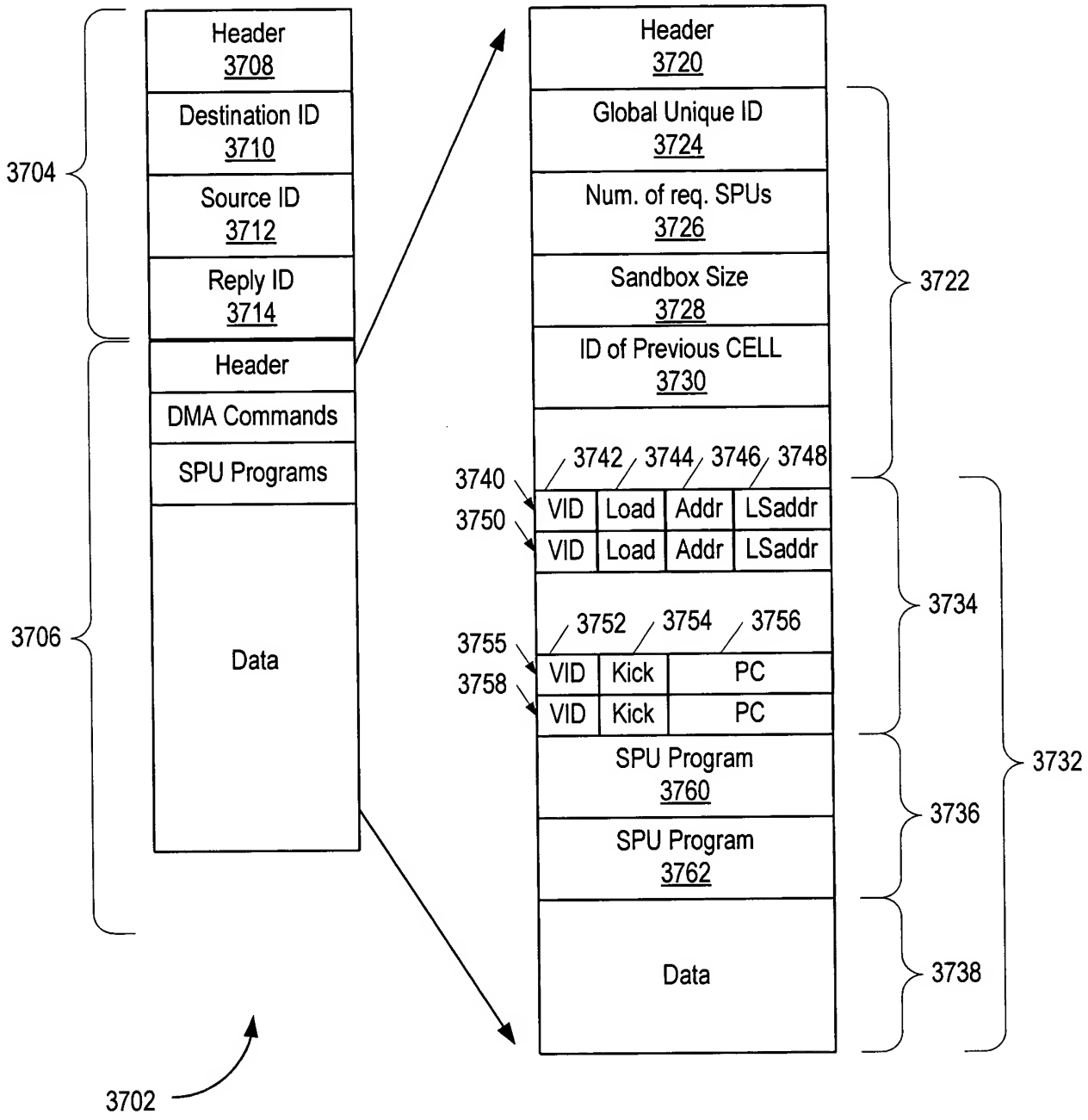
Header
3708
Destination ID
3710
Source ID
3712
Reply ID
3714
Header
DMA Commands
SPU Programs
Data
3704
3706
3702
Header
3720
Global Unique ID
3724
Num. of req. SPUs
3726
Sandbox Size
3728
ID of Previous CELL
3730
3722
3742
3744
3746
3748
3740
VID
Load
Addr
LSaddr
3750
VID
Load
Addr
LSaddr
3734
3752
3754
3756
3755
VID
Kick
PC
3758
VID
Kick
PC
SPU Program
3760
SPU Program
3762
3736
Data
3738
3732

Figure 37

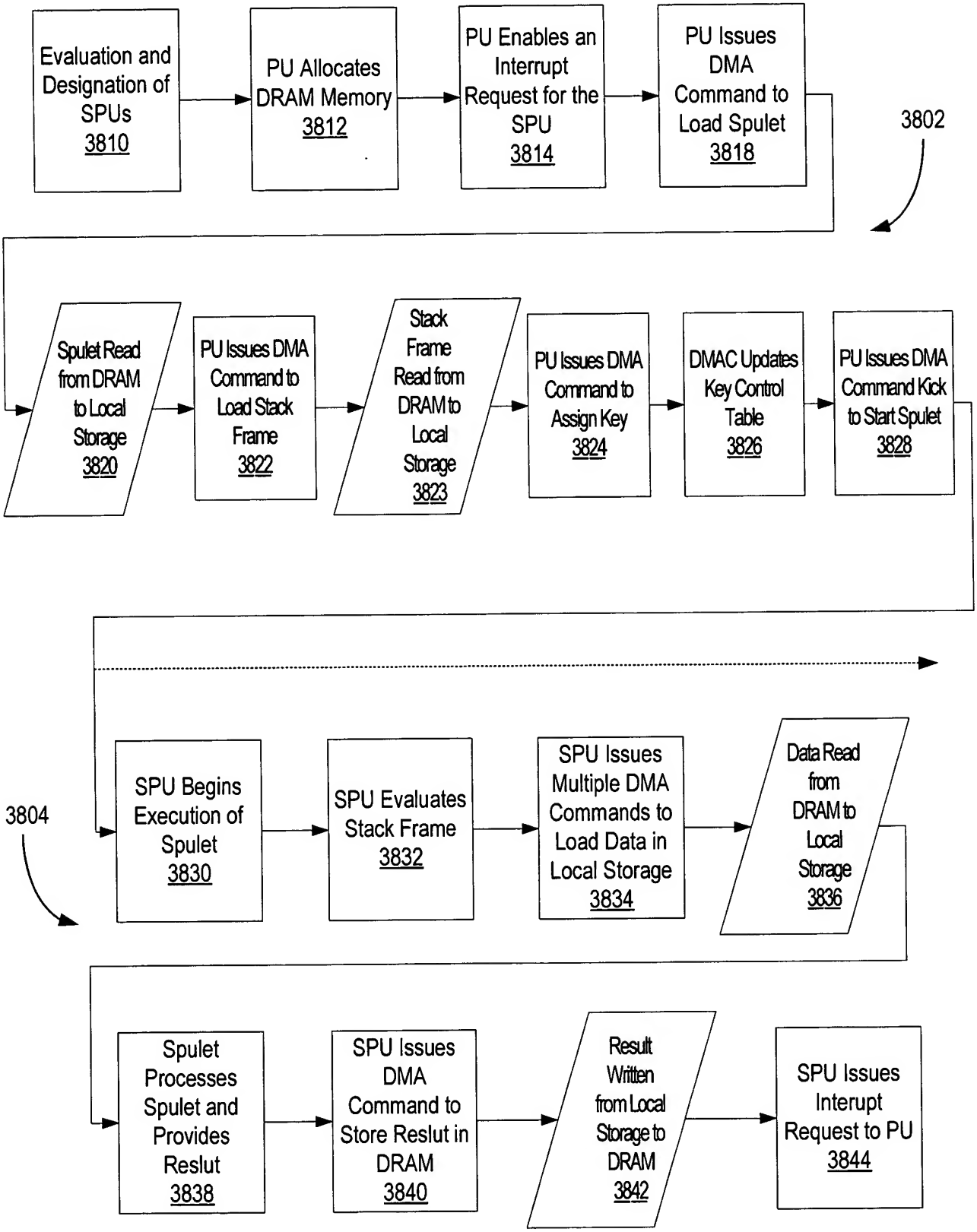
Evaluation and Designation of SPUs 3810
PU Allocates DRAM Memory 3812
PU Enables an Interrupt Request for the SPU 3814
PU Issues DMA Command to Load Spulet 3818
3802
Spulet Read from DRAM to Local Storage 3820
PU Issues DMA Command to Load Stack Frame 3822
Stack Frame Read from DRAM to Local Storage 3823
PU Issues DMA Command to Assign Key 3824
DMAC Updates Key Control Table 3826
PU Issues DMA Command Kick to Start Spulet 3828
3804
SPU Begins Execution of Spulet 3830
SPU Evaluates Stack Frame 3832
SPU Issues Multiple DMA Commands to Load Data in Local Storage 3834
Data Read from DRAM to Local Storage 3836
Spulet Processes Spulet and Provides Reslut 3838
SPU Issues DMA Command to Store Reslut in DRAM 3840
Result Written from Local Storage to DRAM 3842
SPU Issues Interupt Request to PU 3844

Figure 38

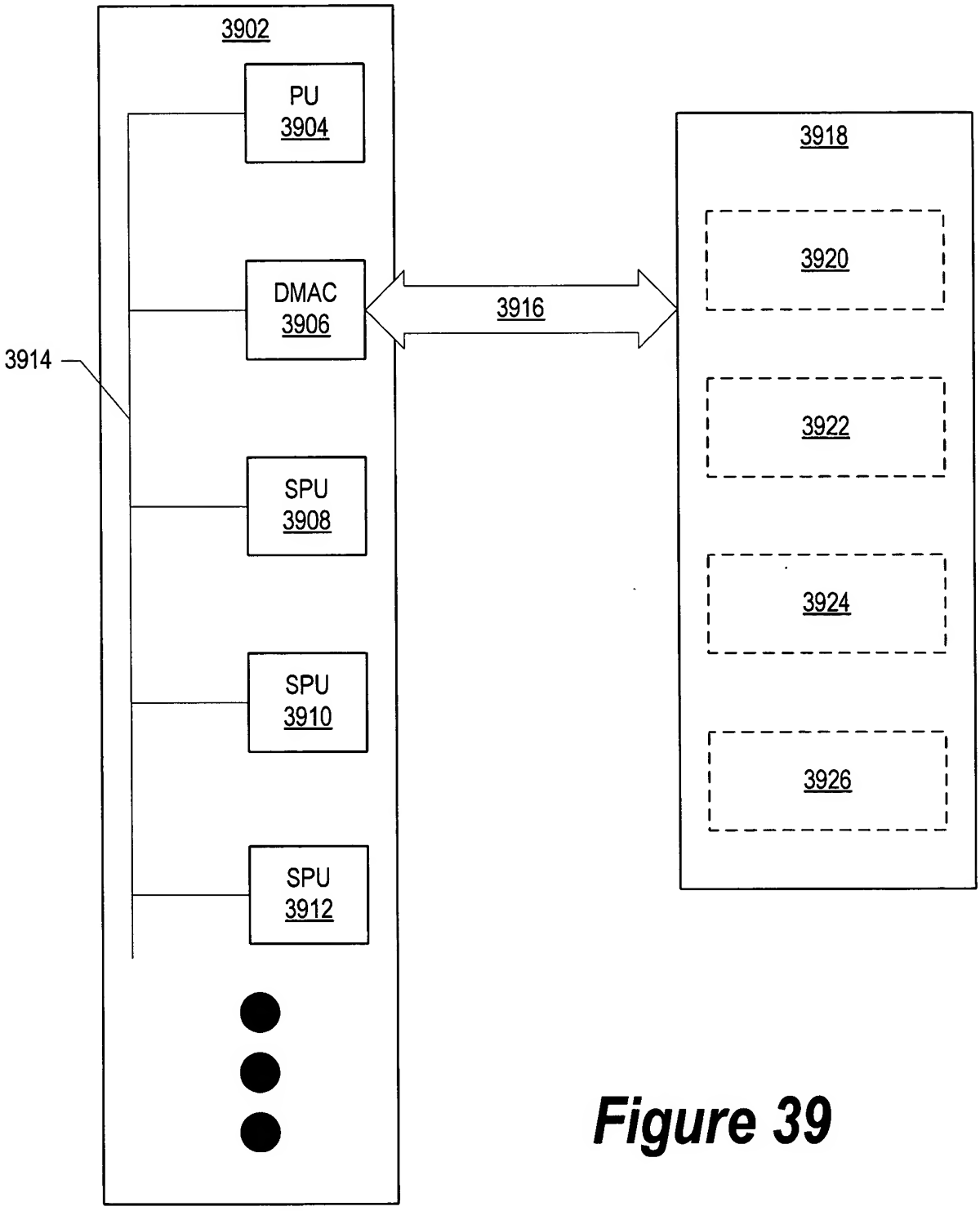
3902
PU
3904
DMAC
3906
3914
SPU
3908
SPU
3910
SPU
3912
3916
3918
3920
3922
3924
3926

Figure 39

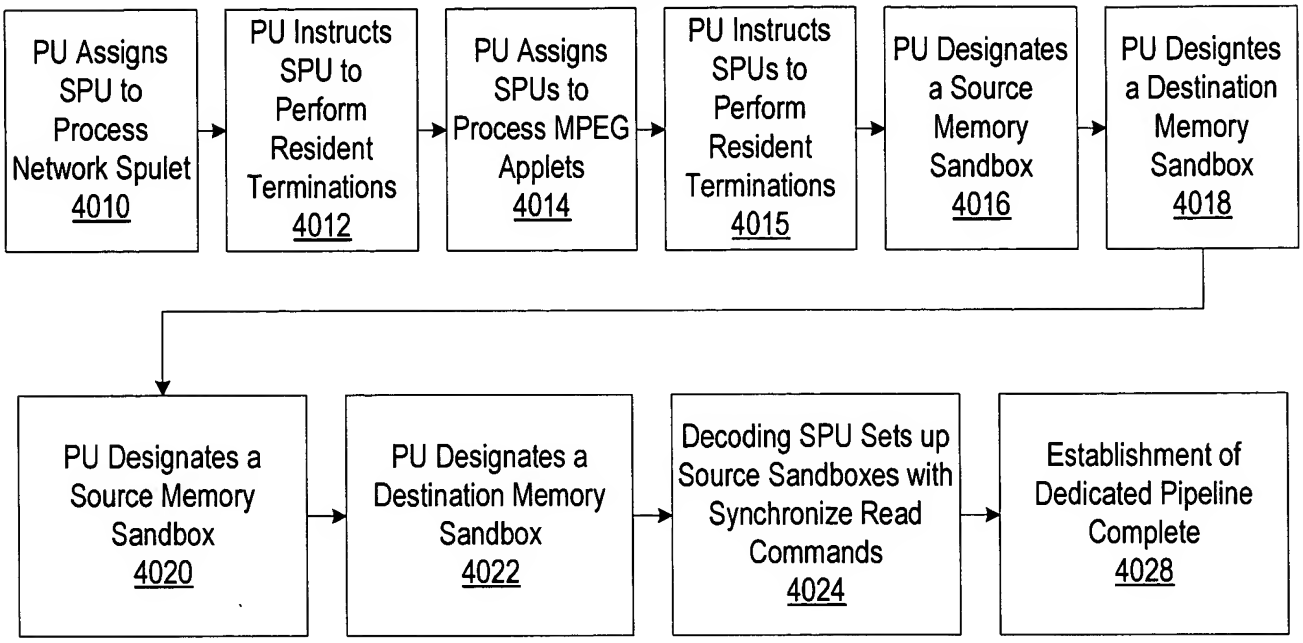

Figure 40A

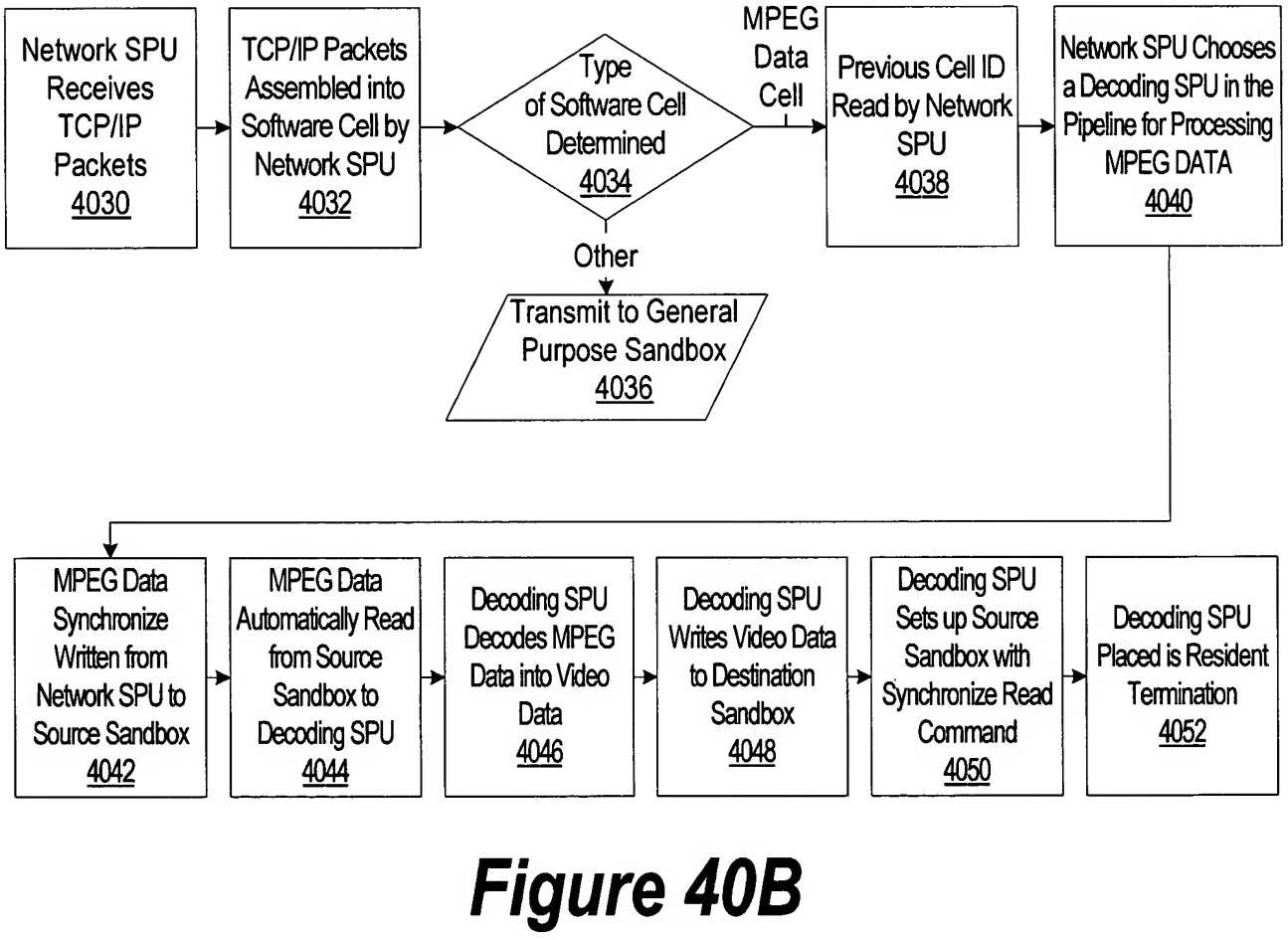

Figure 40B

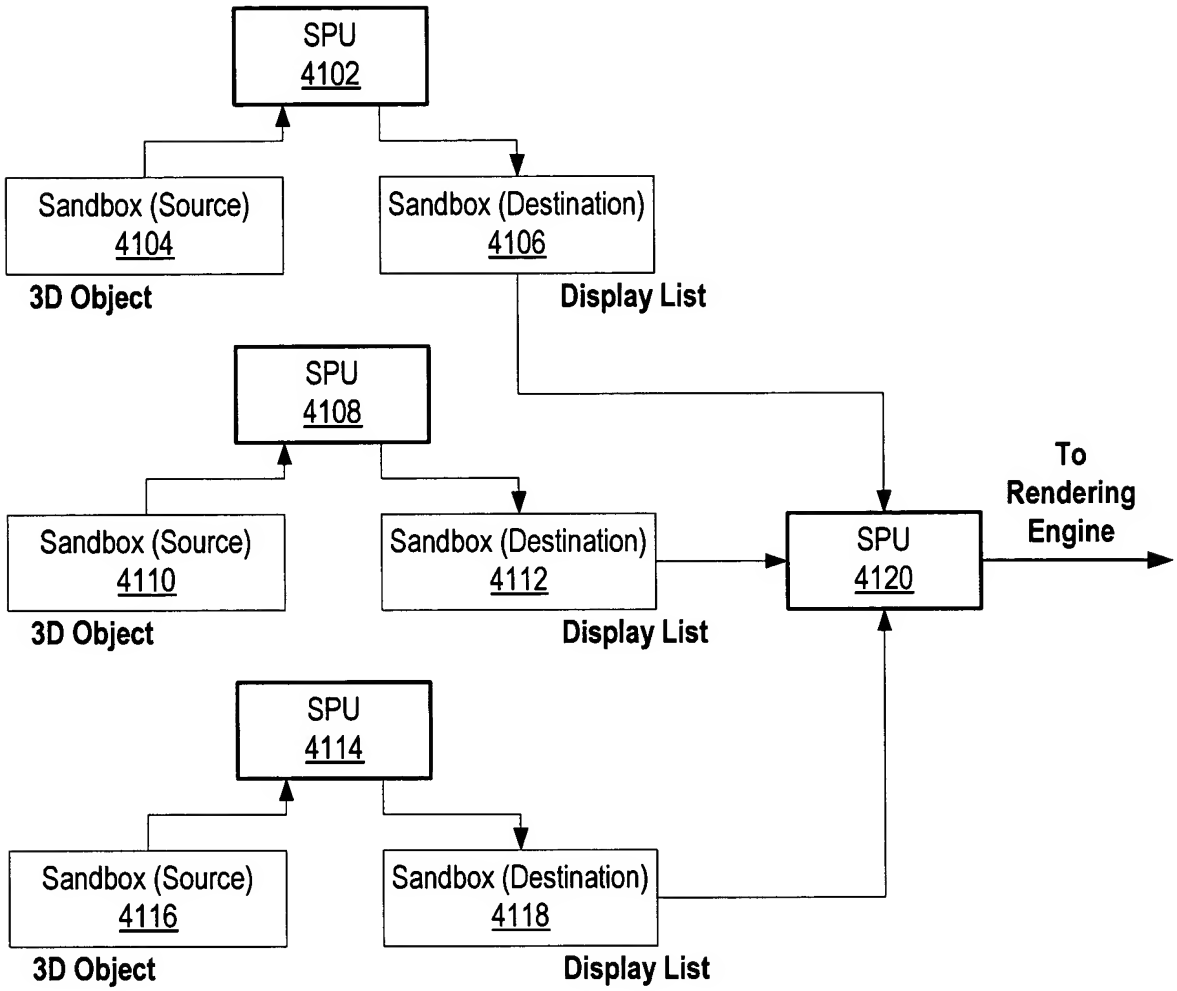
SPU
4102
Sandbox (Source)
4104
3D Object
Sandbox (Destination)
4106
Display List
SPU
4108
Sandbox (Source)
4110
3D Object
Sandbox (Destination)
4112
Display List
SPU
4120
To
Rendering
Engine
SPU
4114
Sandbox (Source)
4116
3D Object
Sandbox (Destination)
4118
Display List

Figure 41

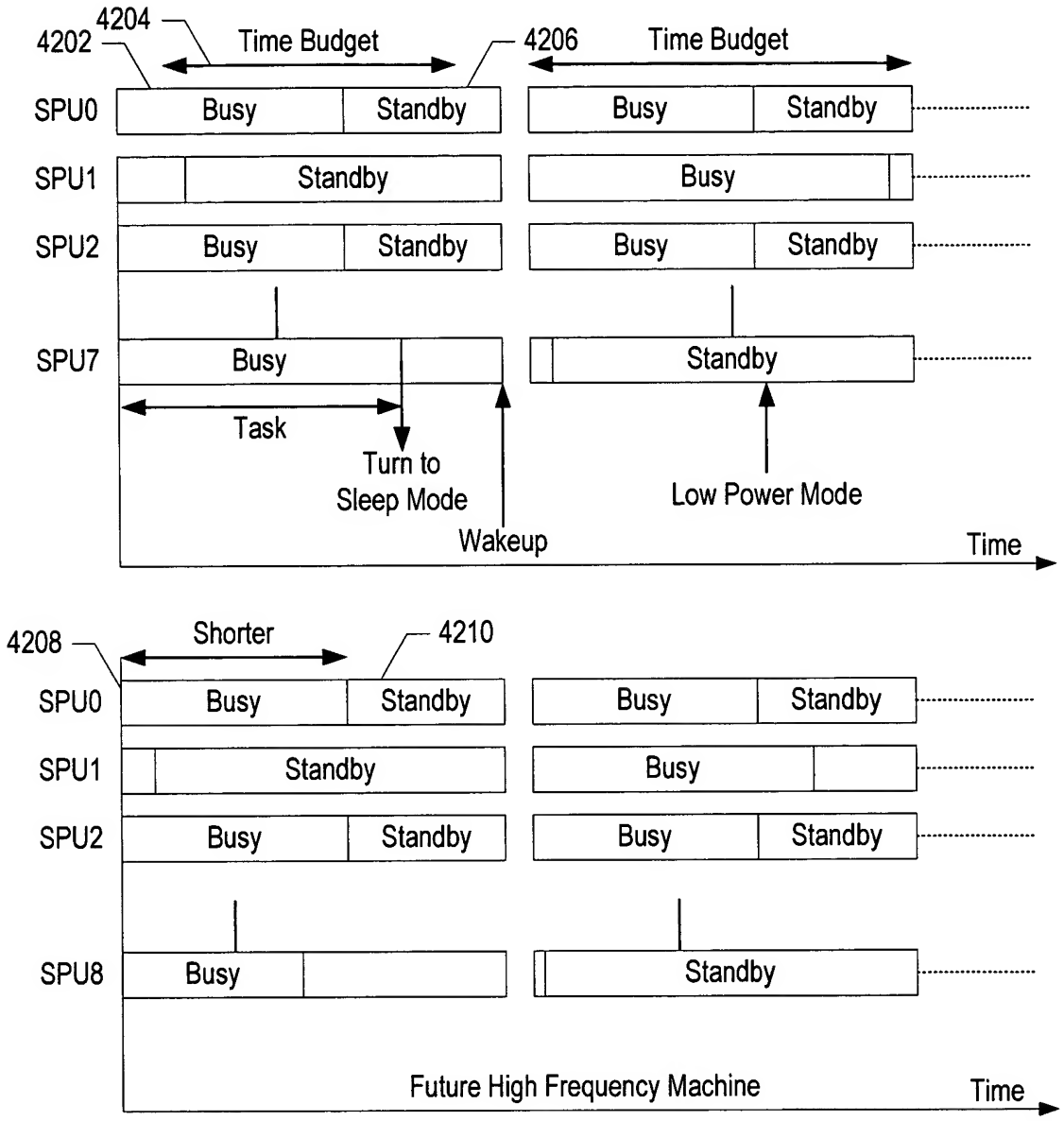
4202
4204
Time Budget
4206
Time Budget
SPU0
Busy
Standby
Busy
Standby
SPU1
Standby
Busy
SPU2
Busy
Standby
Busy
Standby
SPU7
Busy
Standby
Task
Turn to
Sleep Mode
Low Power Mode
Wakeup
Time
4208
Shorter
4210
SPU0
Busy
Standby
Busy
Standby
SPU1
Standby
Busy
SPU2
Busy
Standby
Busy
Standby
SPU8
Busy
Standby
Future High Frequency Machine
Time

Figure 42

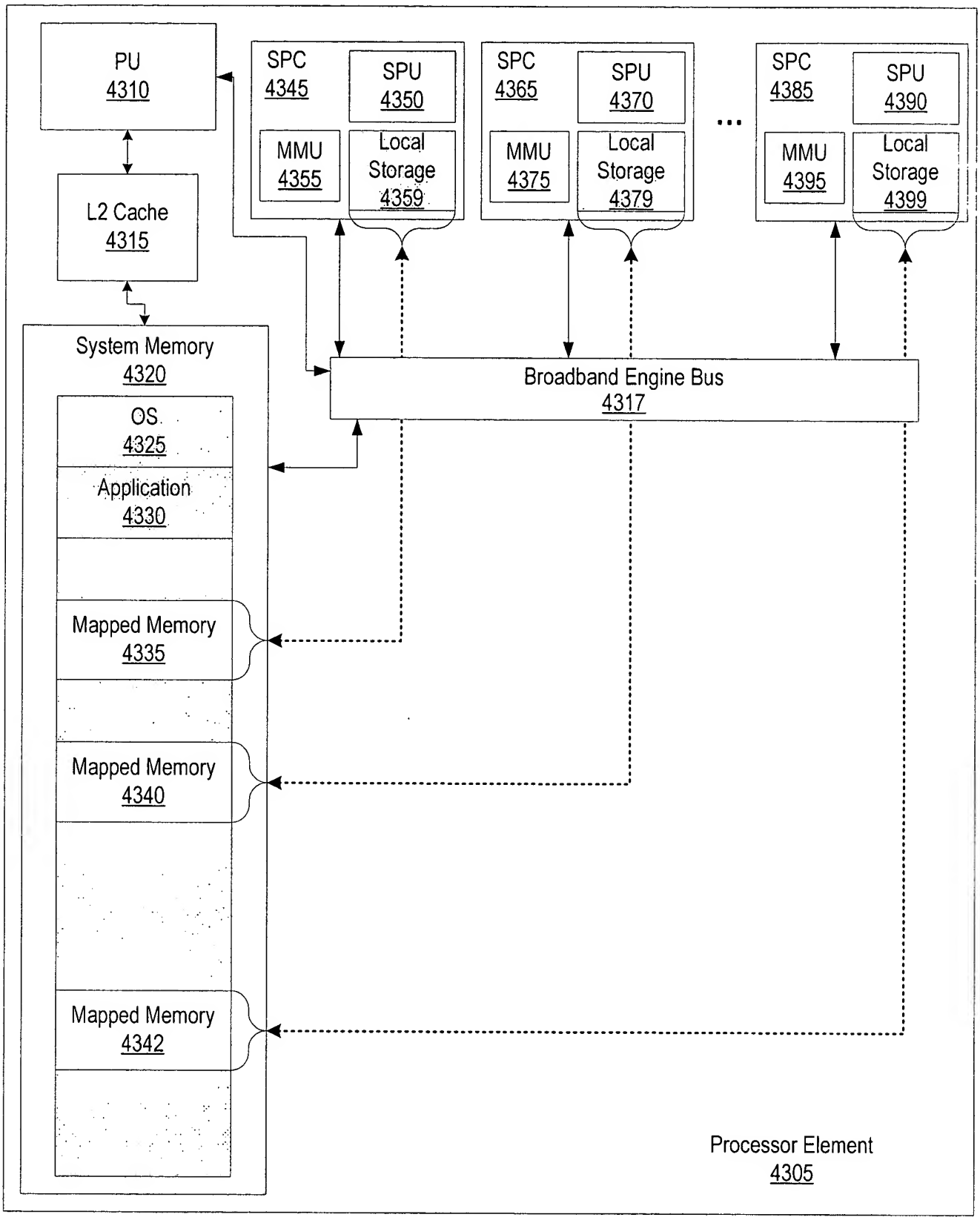
PU
4310
L2 Cache
4315
SPC
4345
SPU
4350
MMU
4355
Local
Storage
4359
SPC
4365
SPU
4370
MMU
4375
Local
Storage
4379
...
SPC
4385
SPU
4390
MMU
4395
Local
Storage
4399
System Memory
4320
Broadband Engine Bus
4317
OS
4325
Application
4330
Mapped Memory
4335
Mapped Memory
4340
Mapped Memory
4342
Processor Element
4305

Figure 43

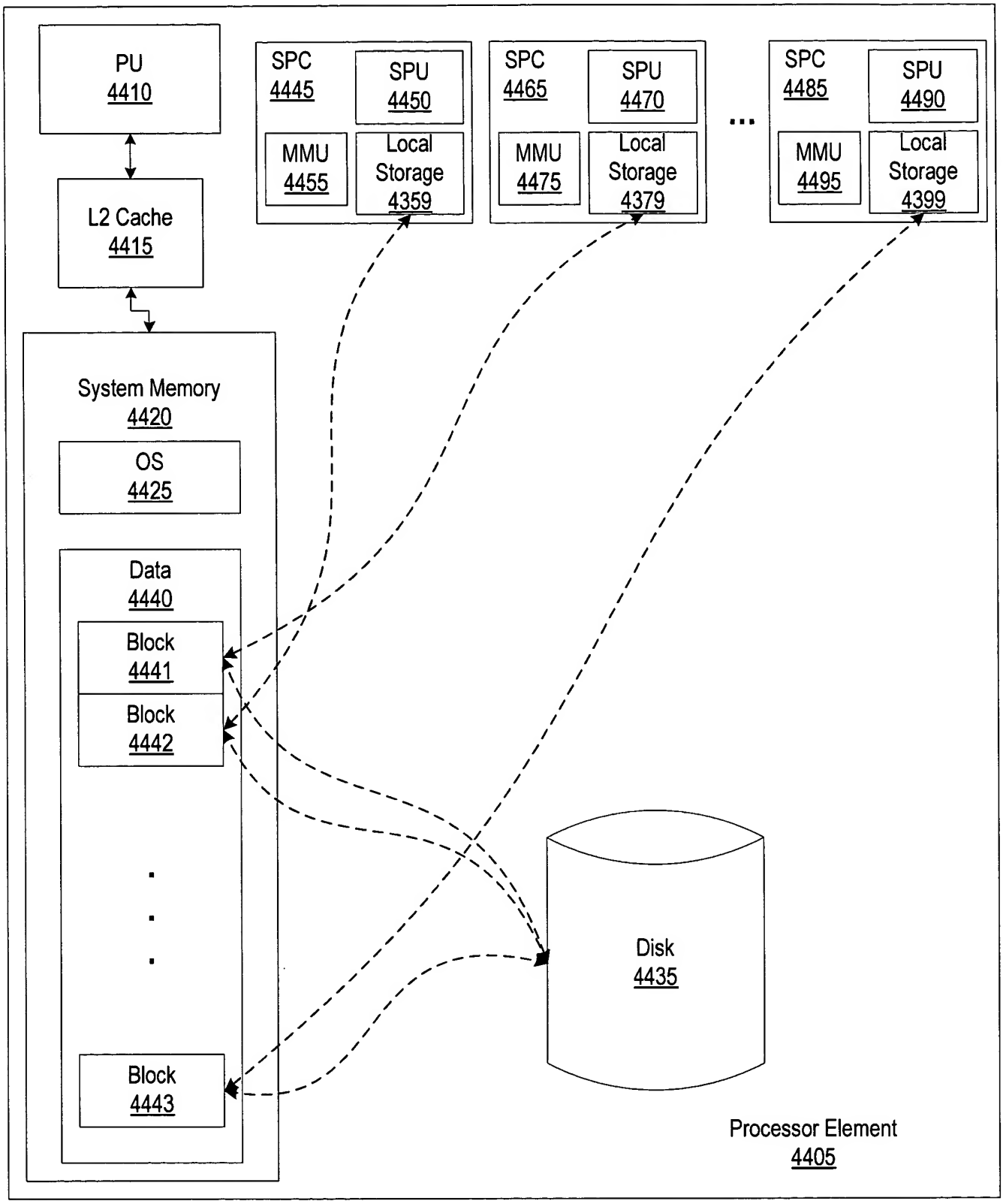
PU
4410
L2 Cache
4415
System Memory
4420
OS
4425
Data
4440
Block
4441
Block
4442
Block
4443
SPC
4445
SPU
4450
MMU
4455
Local Storage
4359
SPC
4465
SPU
4470
MMU
4475
Local Storage
4379
SPC
4485
SPU
4490
MMU
4495
Local Storage
4399
Disk
4435
Processor Element
4405

Figure 44

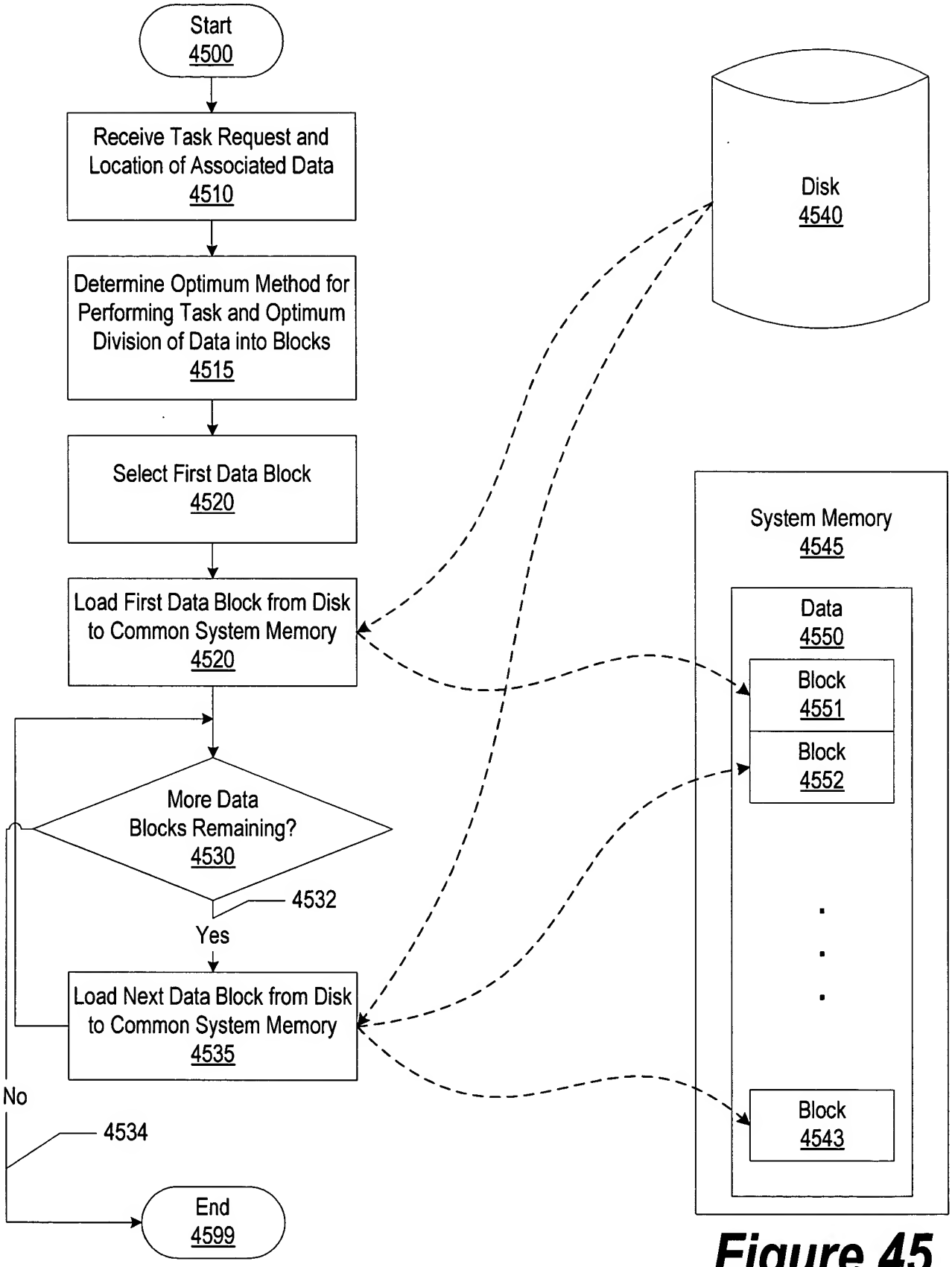
Start
4500
Receive Task Request and Location of Associated Data
4510
Determine Optimum Method for Performing Task and Optimum Division of Data into Blocks
4515
Select First Data Block
4520
Load First Data Block from Disk to Common System Memory
4520
More Data Blocks Remaining?
4530
4532
Yes
Load Next Data Block from Disk to Common System Memory
4535
No
4534
End
4599
Disk
4540
System Memory
4545
Data
4550
Block
4551
Block
4552
Block
4543

Figure 45

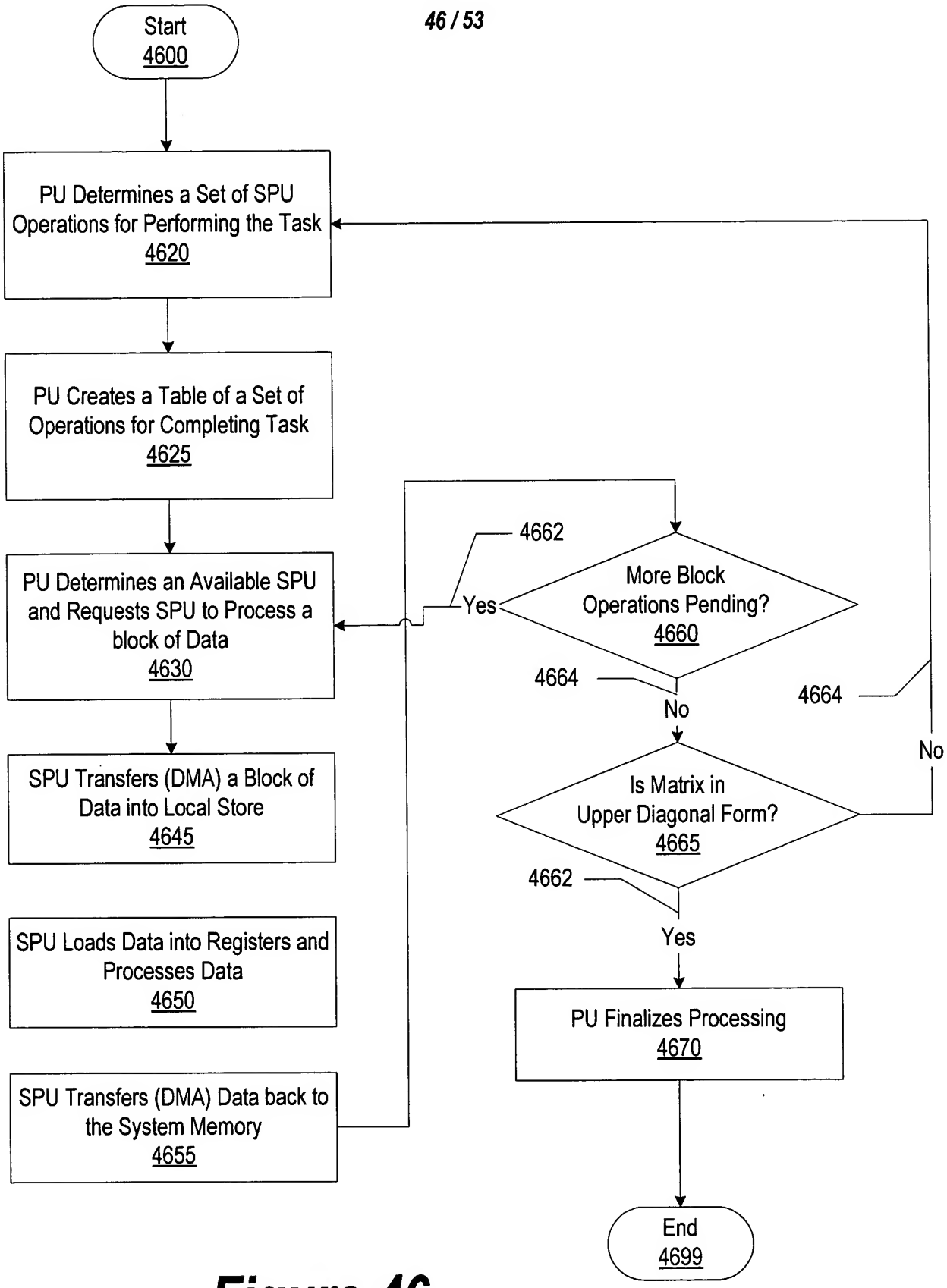
Start
4600
PU Determines a Set of SPU Operations for Performing the Task
4620
PU Creates a Table of a Set of Operations for Completing Task
4625
PU Determines an Available SPU and Requests SPU to Process a block of Data
4630
SPU Transfers (DMA) a Block of Data into Local Store
4645
SPU Loads Data into Registers and Processes Data
4650
SPU Transfers (DMA) Data back to the System Memory
4655
4662
More Block Operations Pending?
4660
Yes
4664
No
4664
No
Is Matrix in Upper Diagonal Form?
4665
4662
Yes
PU Finalizes Processing
4670
End
4699

Figure 46

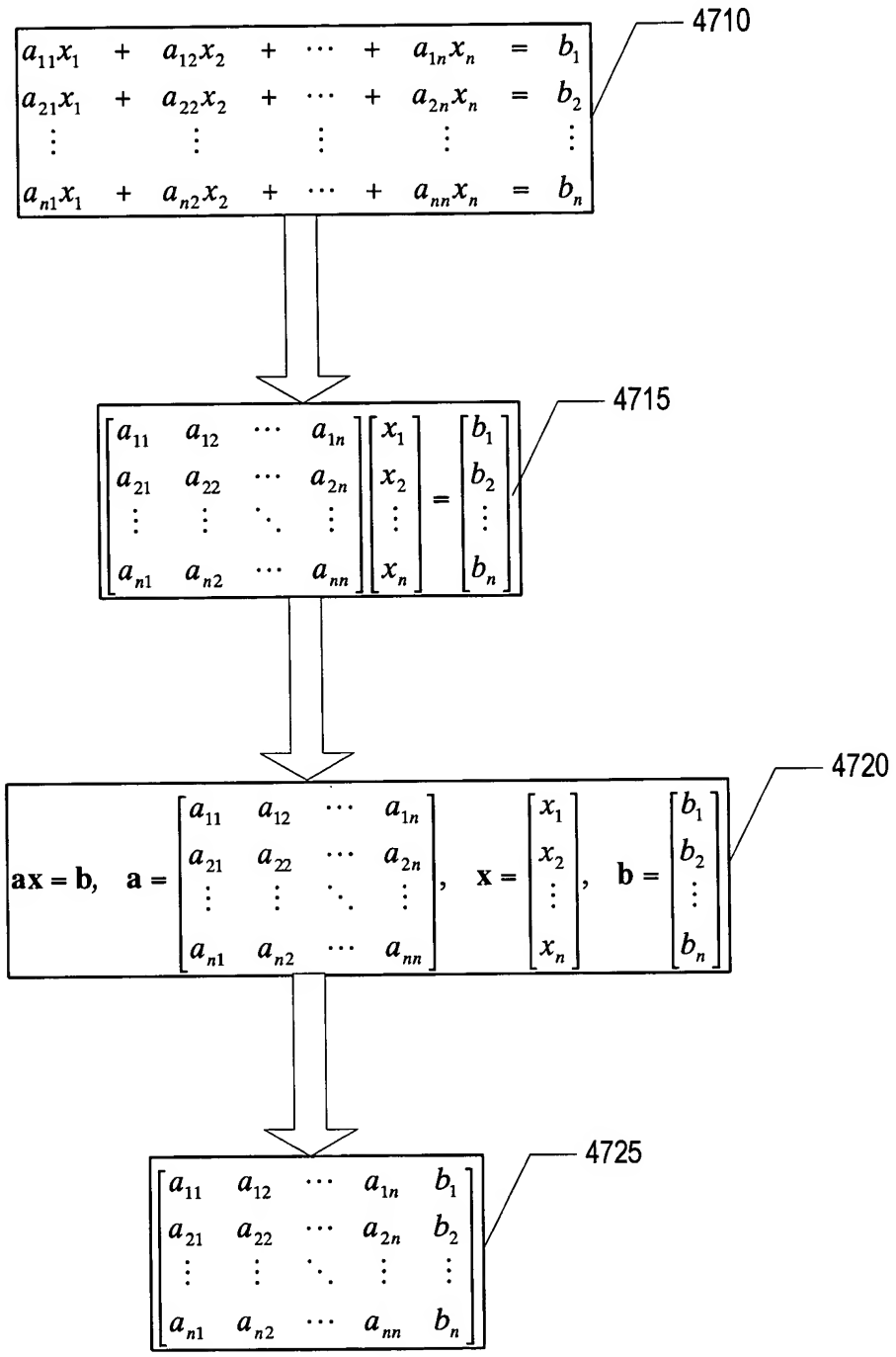

Figure 47

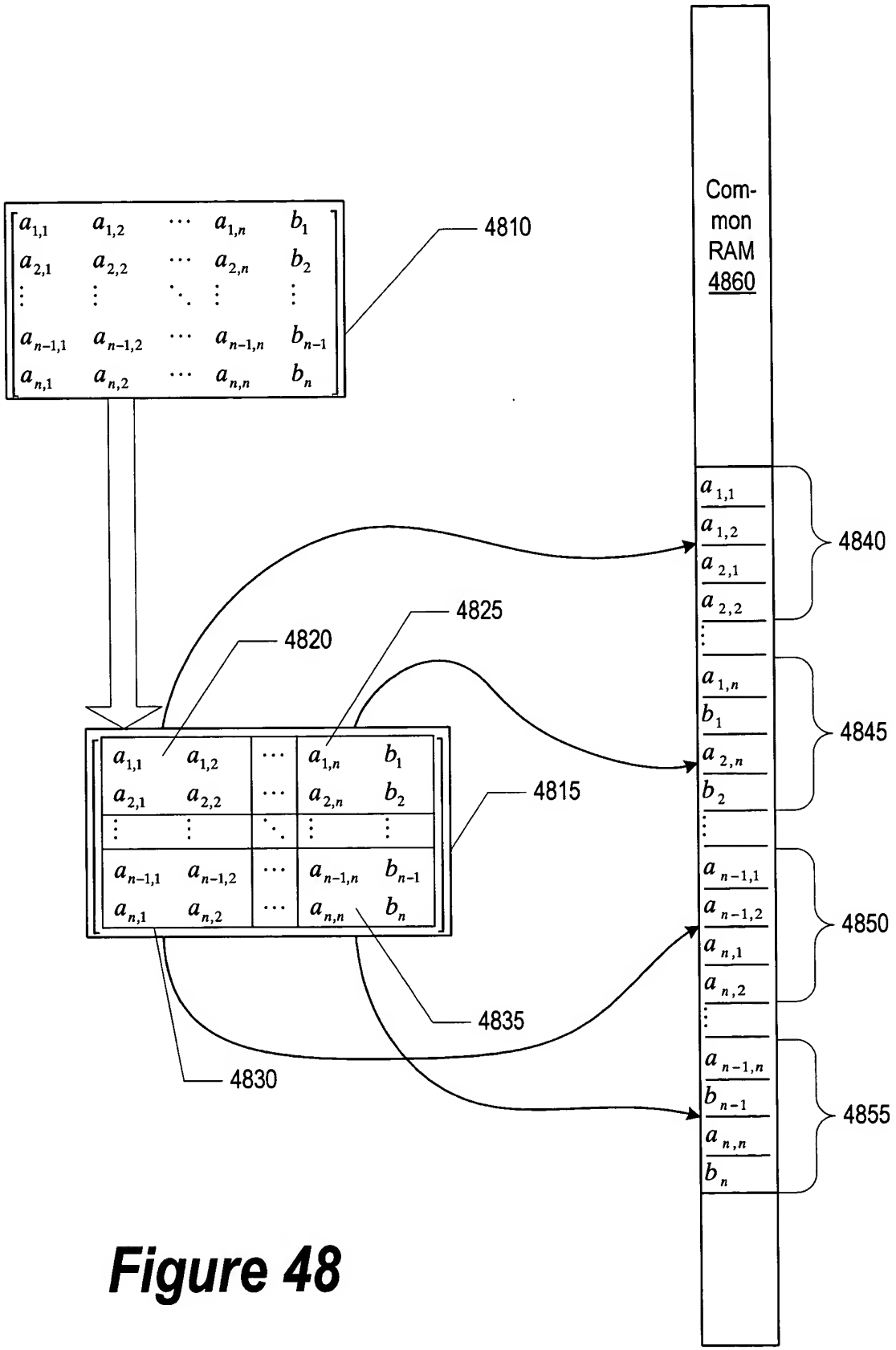
Com-
mon
RAM
4860
4810
4820
4825
4815
4830
4835
4840
4845
4850
4855

Figure 48

Operations	Block Operations	Completed?	SPU
Replace R1 with 4*R1+R2			
	Perform on Block A	Yes	SPU 5
	...	...	...
	Perform on Block Z	In Progress	SPU 2
Replace R5 with 5*R8+			
	Perform on Block ...	No	?

4900

Figure 49

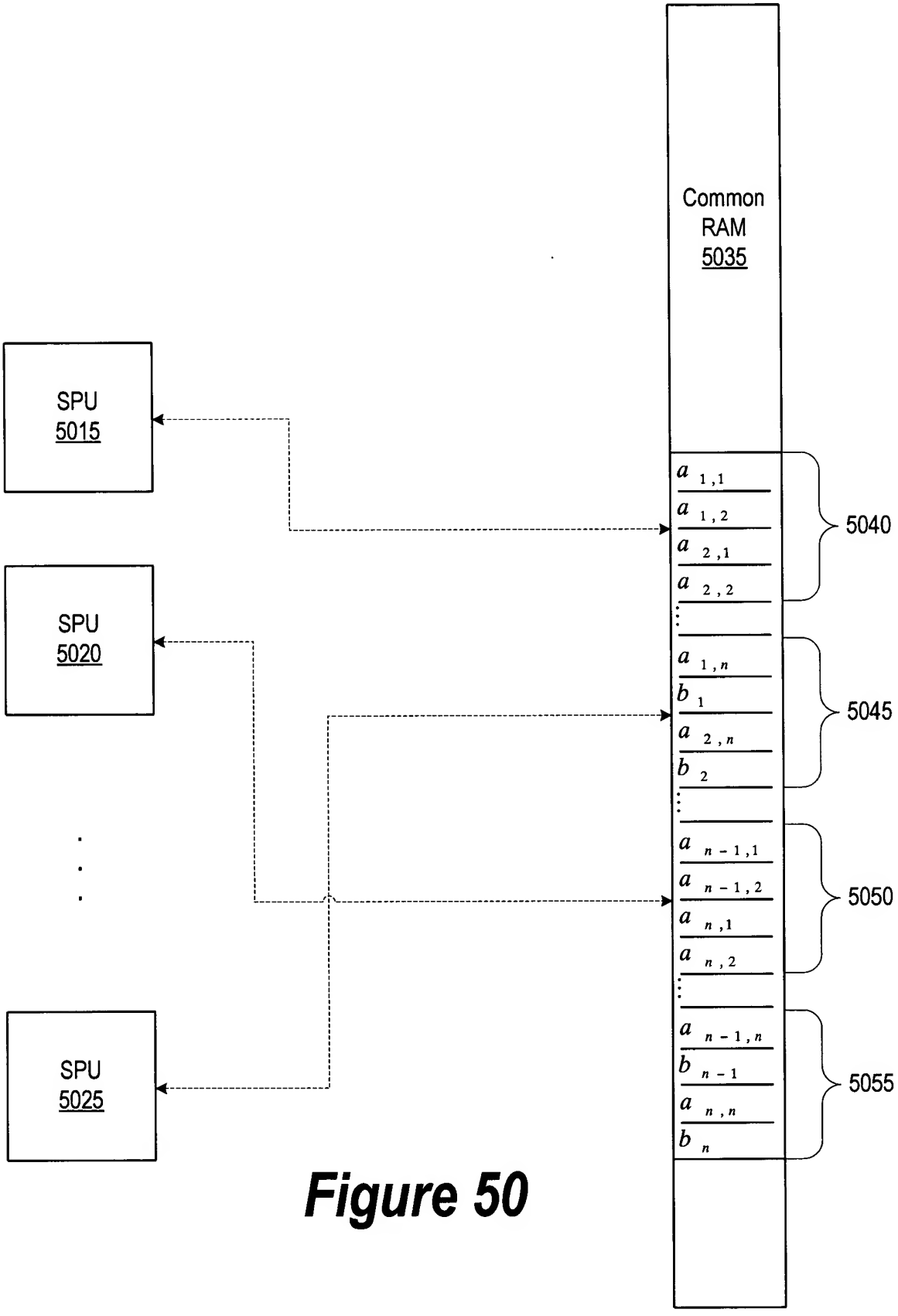
Common
RAM
5035
SPU
5015
SPU
5020
SPU
5025
$a_{1,1}$
$a_{1,2}$
$a_{2,1}$
$a_{2,2}$
$a_{1,n}$
b_1
$a_{2,n}$
b_2
$a_{n-1,1}$
$a_{n-1,2}$
$a_{n,1}$
$a_{n,2}$
$a_{n-1,n}$
b_{n-1}
$a_{n,n}$
b_n
5040
5045
5050
5055

Figure 50

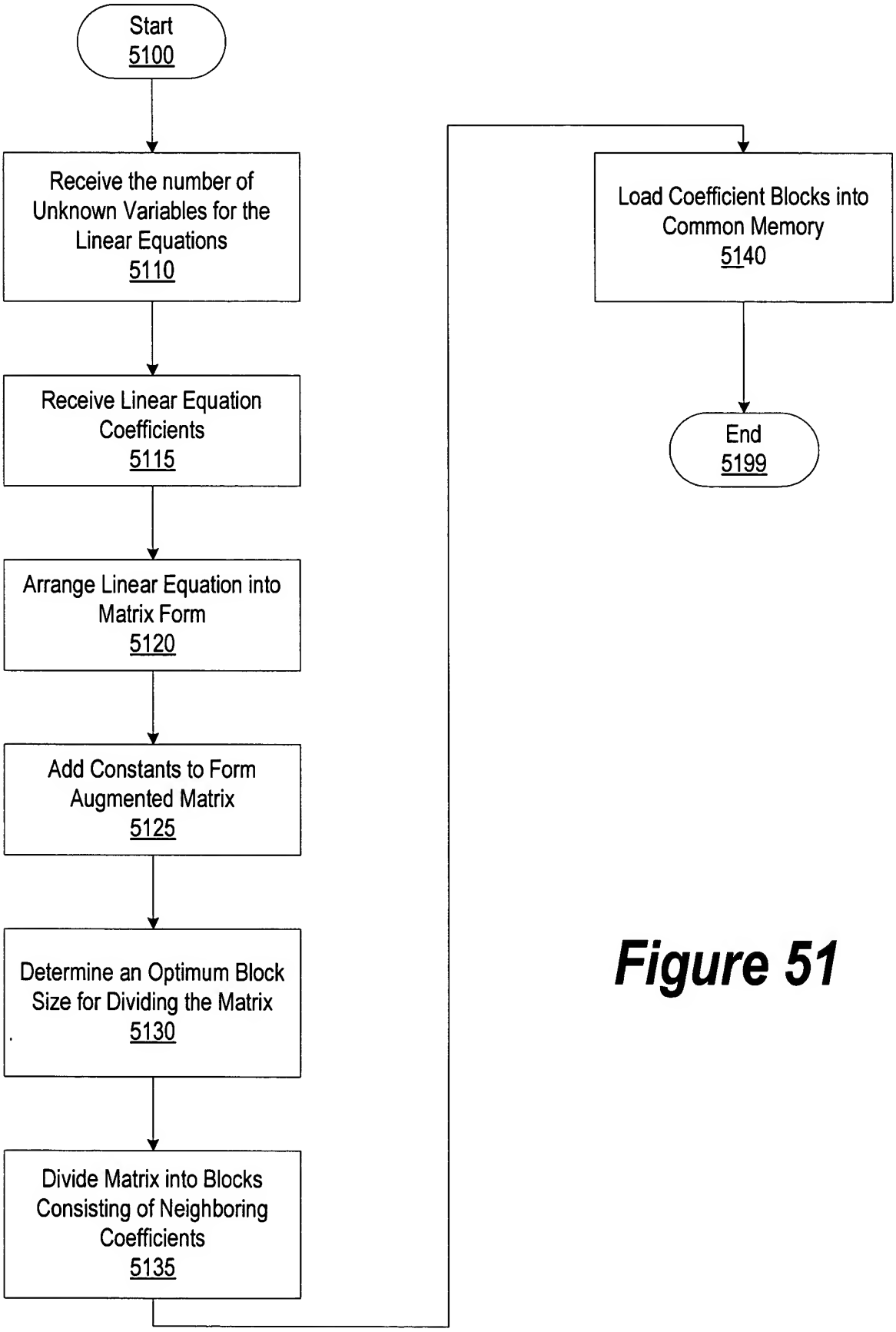
Start
5100
Receive the number of Unknown Variables for the Linear Equations
5110
Receive Linear Equation Coefficients
5115
Arrange Linear Equation into Matrix Form
5120
Add Constants to Form Augmented Matrix
5125
Determine an Optimum Block Size for Dividing the Matrix
5130
Divide Matrix into Blocks Consisting of Neighboring Coefficients
5135
Load Coefficient Blocks into Common Memory
5140
End
5199

Figure 51

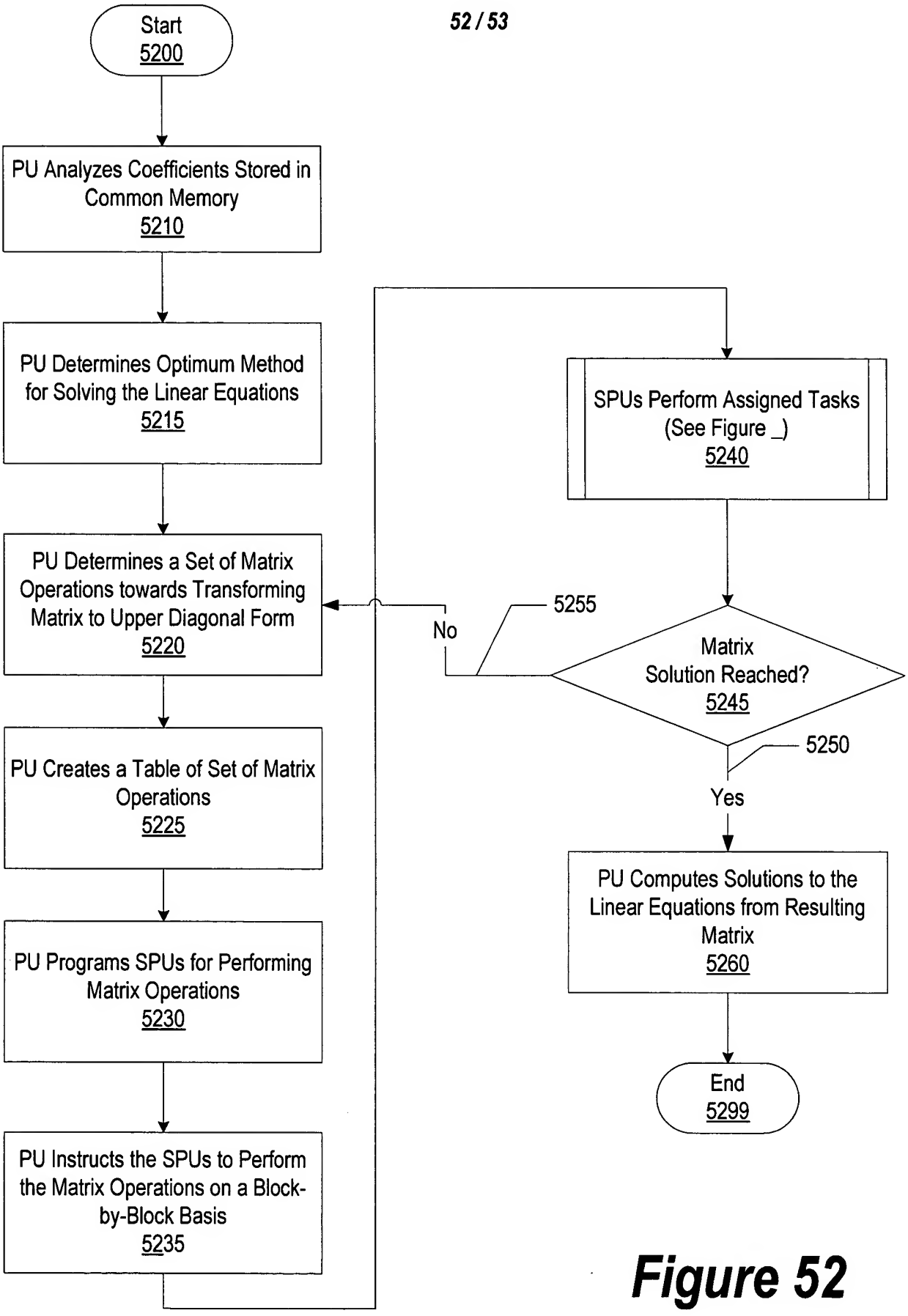
Start
5200
PU Analyzes Coefficients Stored in Common Memory
5210
PU Determines Optimum Method for Solving the Linear Equations
5215
PU Determines a Set of Matrix Operations towards Transforming Matrix to Upper Diagonal Form
5220
PU Creates a Table of Set of Matrix Operations
5225
PU Programs SPUs for Performing Matrix Operations
5230
PU Instructs the SPUs to Perform the Matrix Operations on a Block-by-Block Basis
5235
SPUs Perform Assigned Tasks (See Figure _)
5240
Matrix Solution Reached?
5245
5255
No
5250
Yes
PU Computes Solutions to the Linear Equations from Resulting Matrix
5260
End
5299

Figure 52

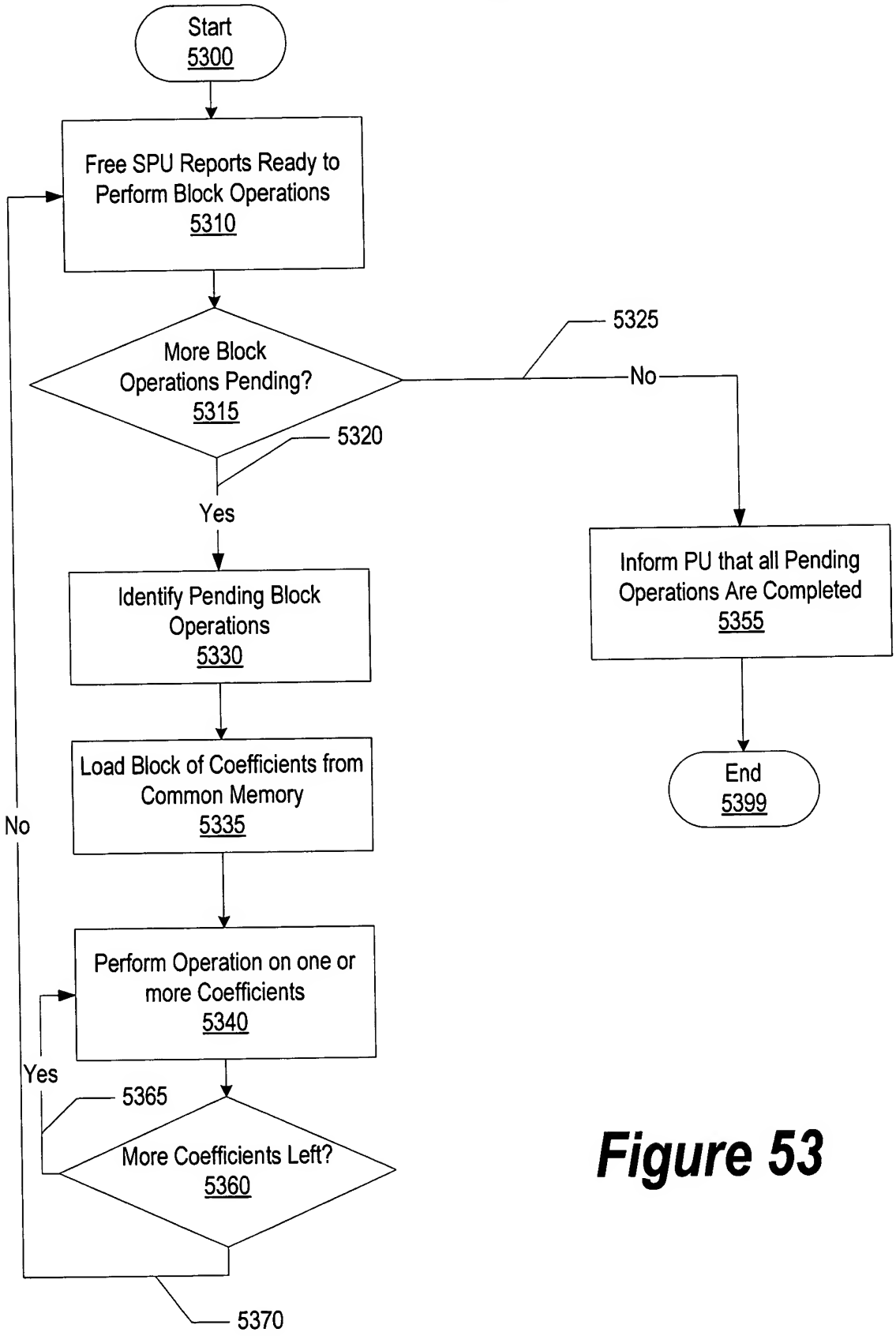
Start
5300
Free SPU Reports Ready to Perform Block Operations
5310
More Block Operations Pending?
5315
5325
No
5320
Yes
Identify Pending Block Operations
5330
Load Block of Coefficients from Common Memory
5335
Perform Operation on one or more Coefficients
5340
More Coefficients Left?
5360
5365
Yes
No
5370
Inform PU that all Pending Operations Are Completed
5355
End
5399

Figure 53